FIG.1

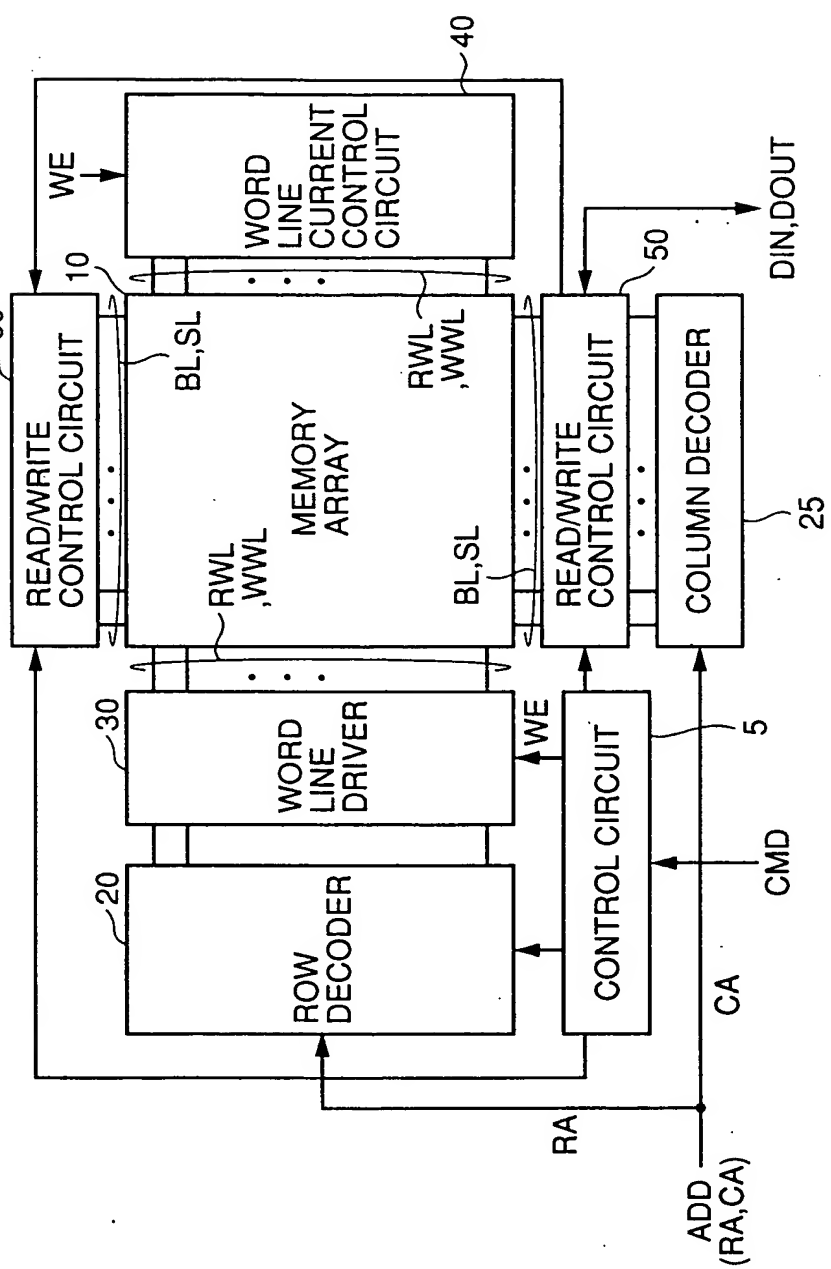
1
40
WE
WORD LINE CURRENT CONTROL CIRCUIT
10
60
READ/WRITE CONTROL CIRCUIT
BL,SL
RWL ,WWL
MEMORY ARRAY
RWL ,WWL
BL,SL
READ/WRITE CONTROL CIRCUIT
50
DIN,DOUT
COLUMN DECODER
25
30
WORD LINE DRIVER
WE
CONTROL CIRCUIT
5
CMD
20
ROW DECODER
CA
RA
ADD (RA,CA)

FIG.2

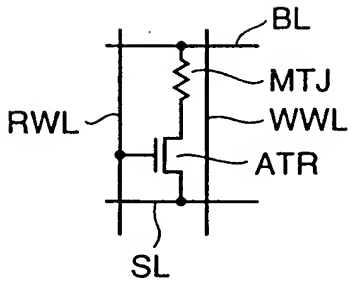
BL
MTJ
RWL
WWL
ATR
SL

FIG.3

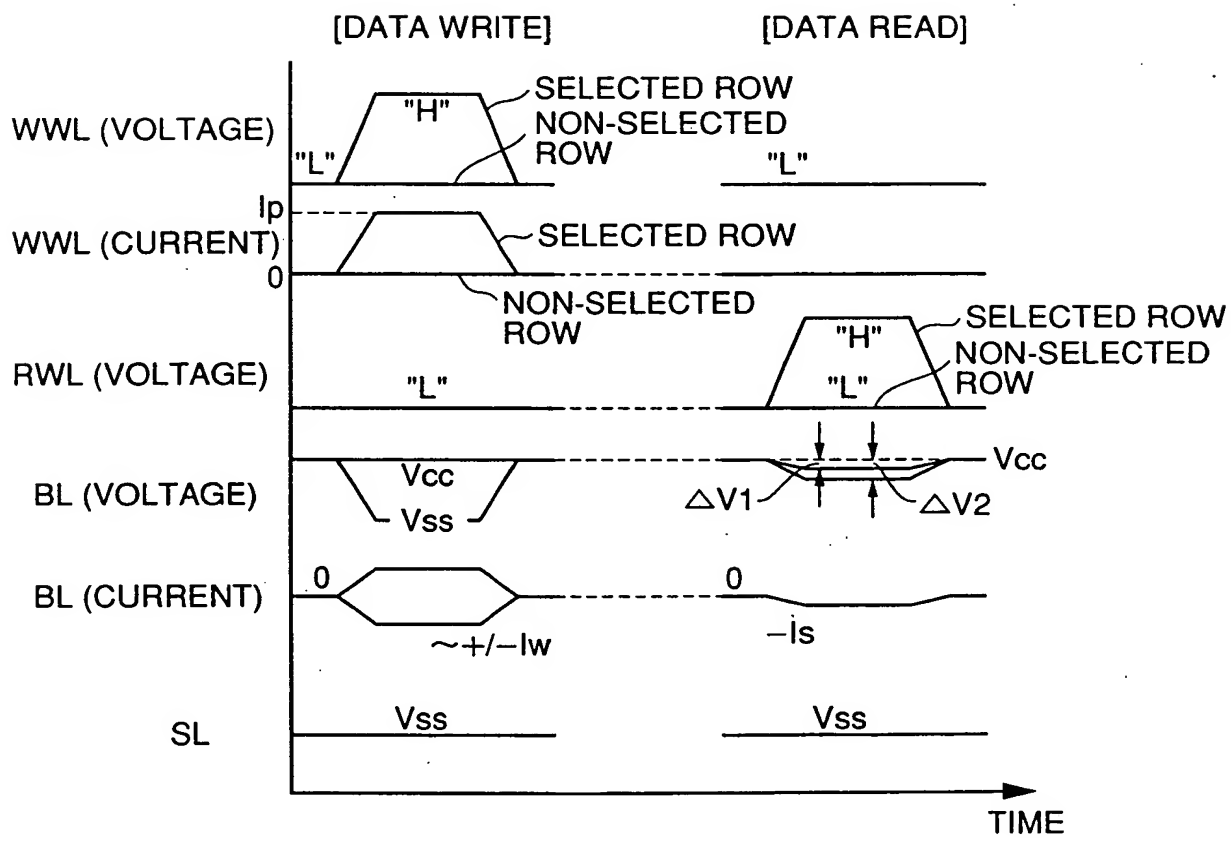
[DATA WRITE]
[DATA READ]
WWL (VOLTAGE)
"H"
"L"
SELECTED ROW
NON-SELECTED ROW
"L"
Ip
WWL (CURRENT)
0
SELECTED ROW
NON-SELECTED ROW
RWL (VOLTAGE)
"H"
"L"
"L"
SELECTED ROW
NON-SELECTED ROW
BL (VOLTAGE)
Vcc
Vss
Vcc
△V1
△V2
BL (CURRENT)
0
0
~+/−Iw
−Is
SL
Vss
Vss
TIME

FIG.4

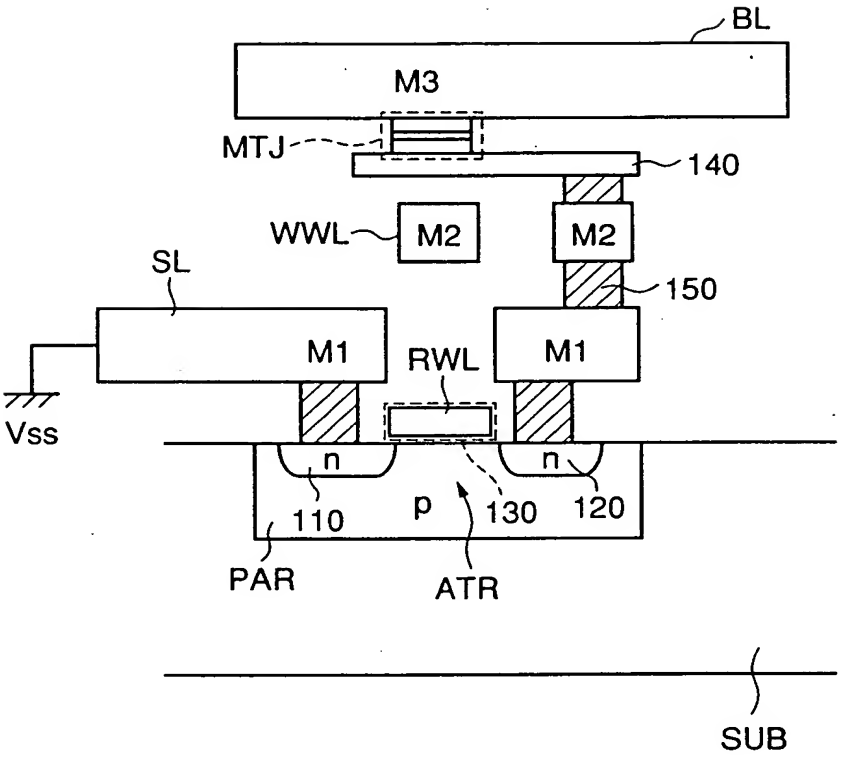
BL
M3
MTJ
140
WWL
M2
M2
SL
150
M1
RWL
M1
Vss
n
n
110
p
130
120
PAR
ATR
SUB

FIG.5

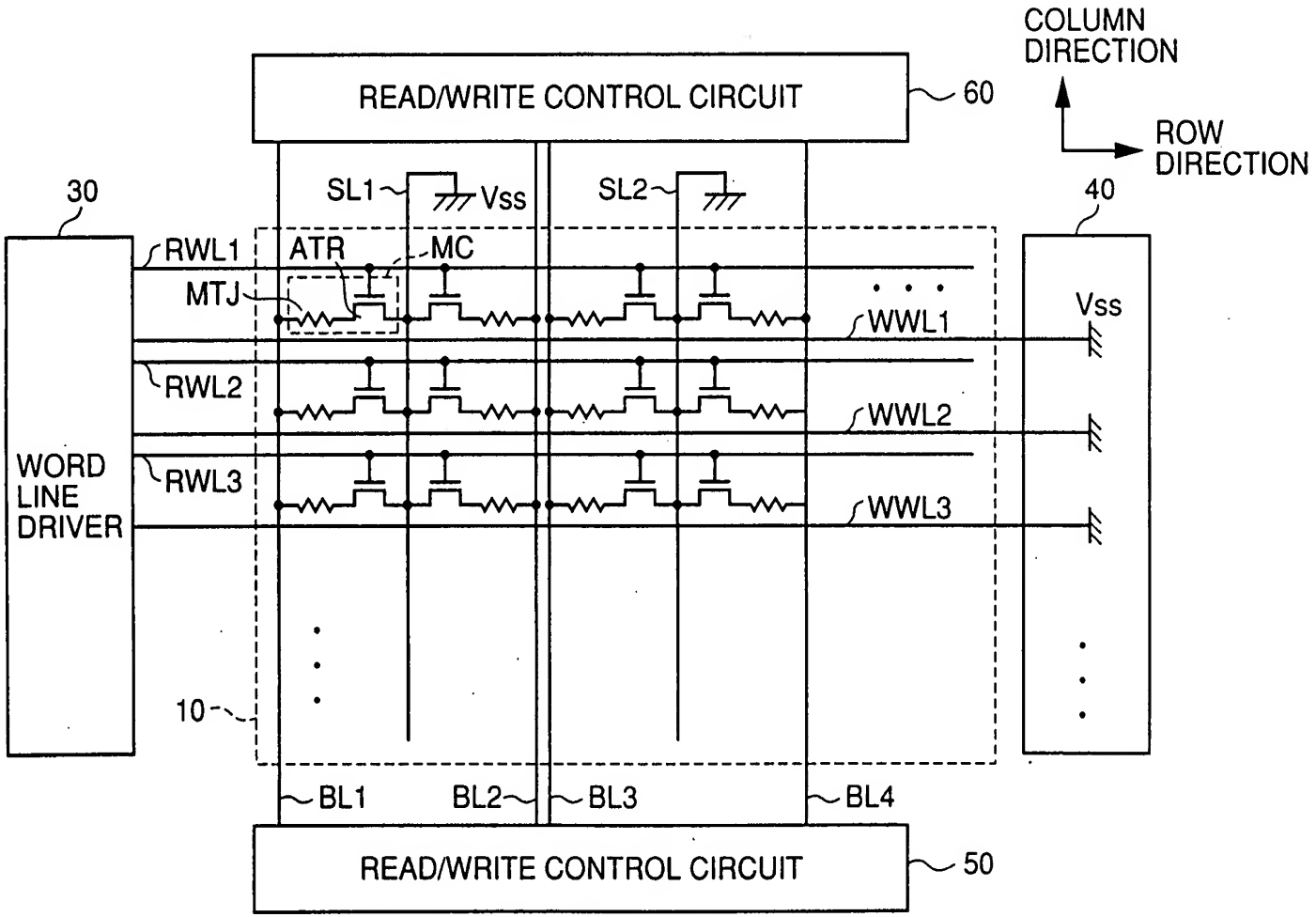
COLUMN DIRECTION
ROW DIRECTION
READ/WRITE CONTROL CIRCUIT
60
30
40
SL1
Vss
SL2
RWL1
ATR
MC
MTJ
WWL1
Vss
RWL2
WWL2
WORD LINE DRIVER
RWL3
WWL3
10
BL1
BL2
BL3
BL4
READ/WRITE CONTROL CIRCUIT
50

FIG.6

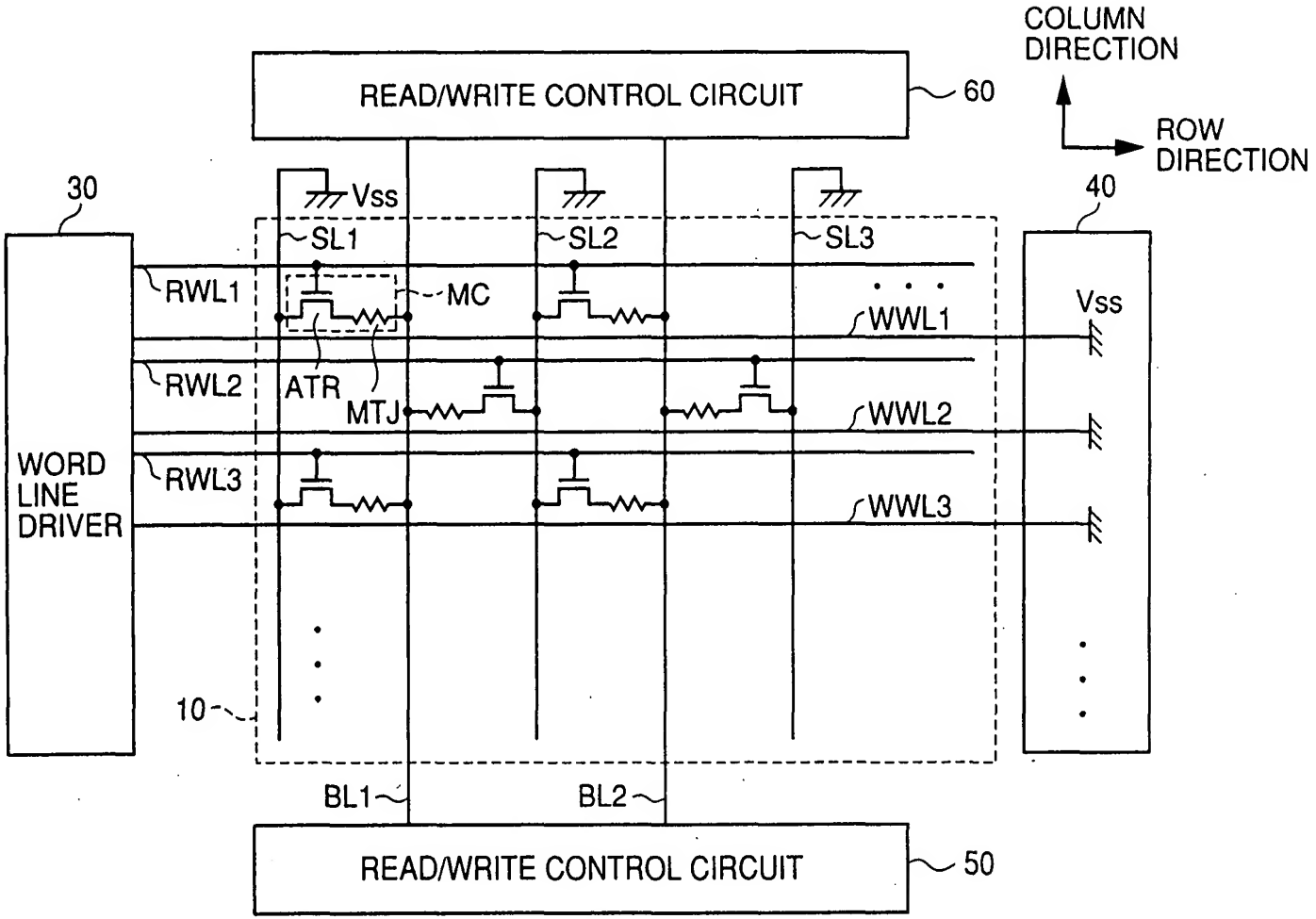
COLUMN DIRECTION
ROW DIRECTION
READ/WRITE CONTROL CIRCUIT
60
30
40
Vss
SL1
SL2
SL3
RWL1
MC
WWL1
Vss
RWL2
ATR
MTJ
WWL2
WORD LINE DRIVER
RWL3
WWL3
10
BL1
BL2
READ/WRITE CONTROL CIRCUIT
50

FIG.7

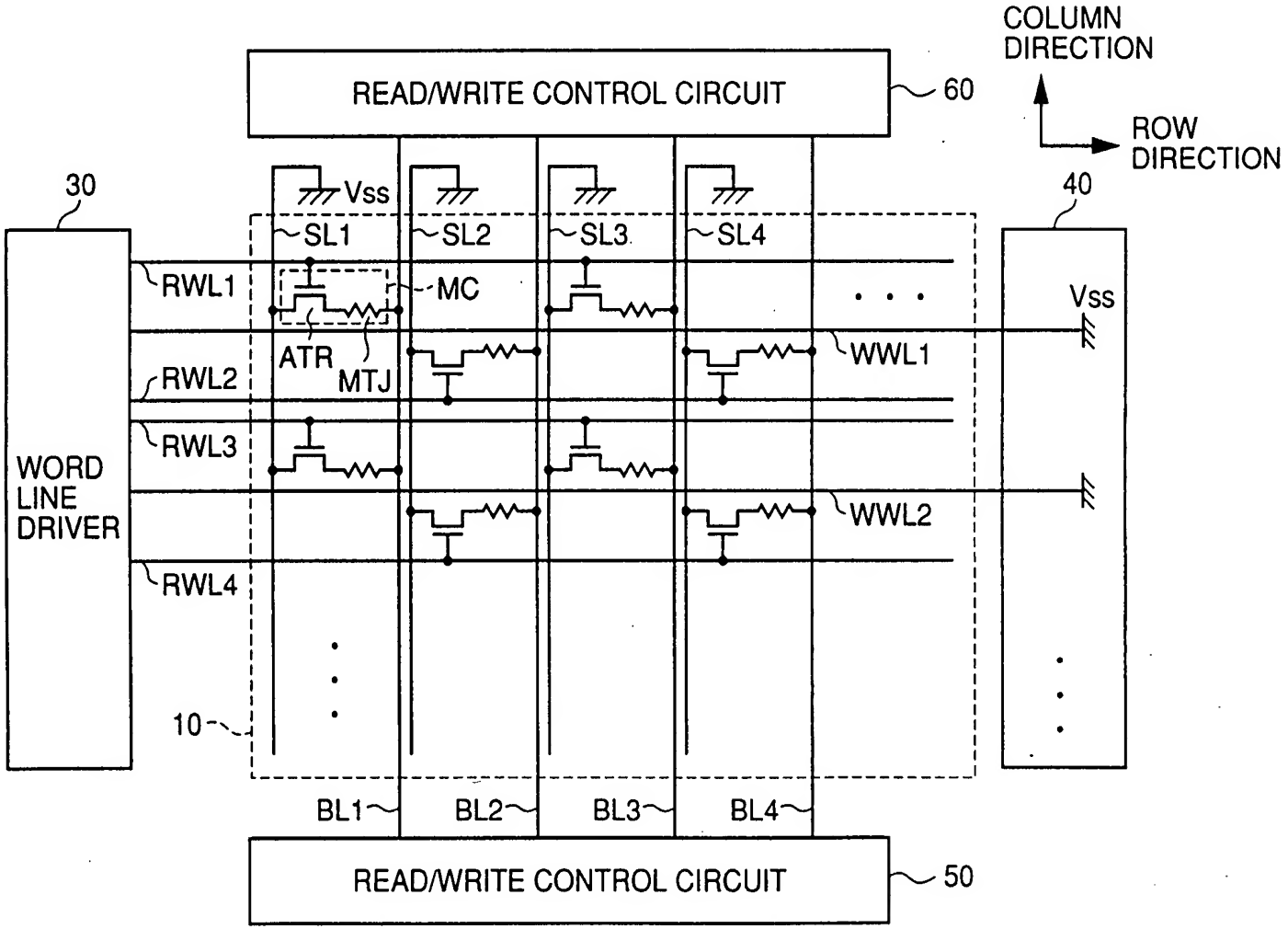
COLUMN DIRECTION
ROW DIRECTION
READ/WRITE CONTROL CIRCUIT
60
30
40
Vss
SL1
SL2
SL3
SL4
RWL1
MC
ATR
MTJ
RWL2
RWL3
RWL4
WWL1
WWL2
WORD LINE DRIVER
10
BL1
BL2
BL3
BL4
READ/WRITE CONTROL CIRCUIT
50

FIG.8A

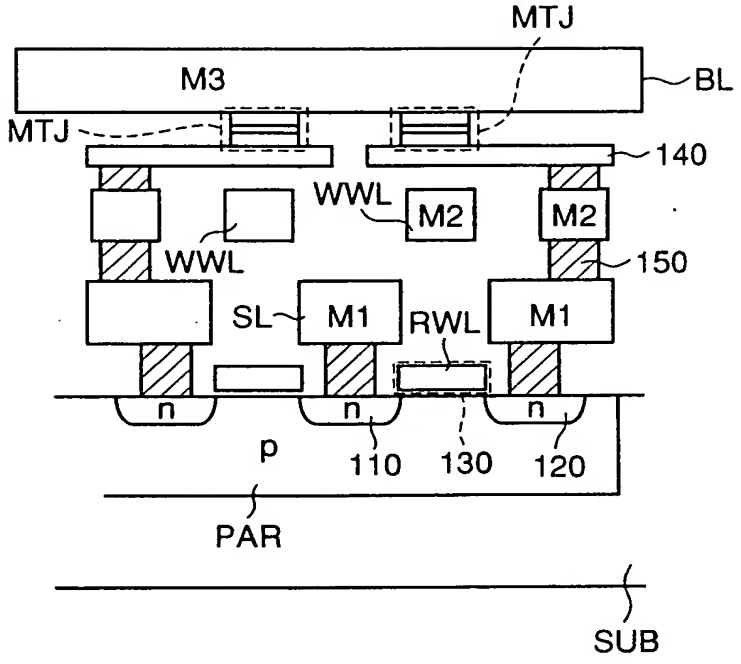
MTJ
M3
BL
MTJ
140
WWL
M2
M2
WWL
150
SL
M1
RWL
M1
n
n
n
p
110
130
120
PAR
SUB

FIG.8B

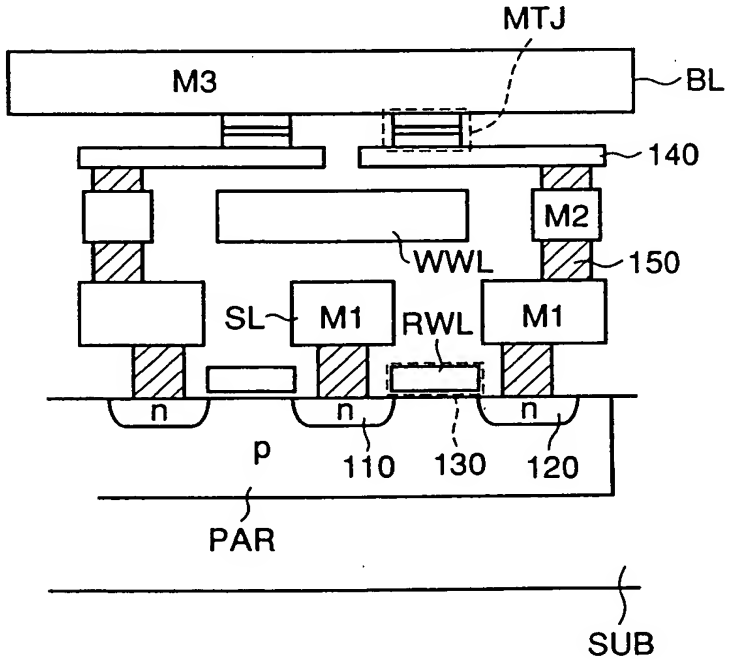
MTJ
M3
BL
140
M2
WWL
150
SL
M1
RWL
M1
n
n
n
p
110
130
120
PAR
SUB

FIG.9

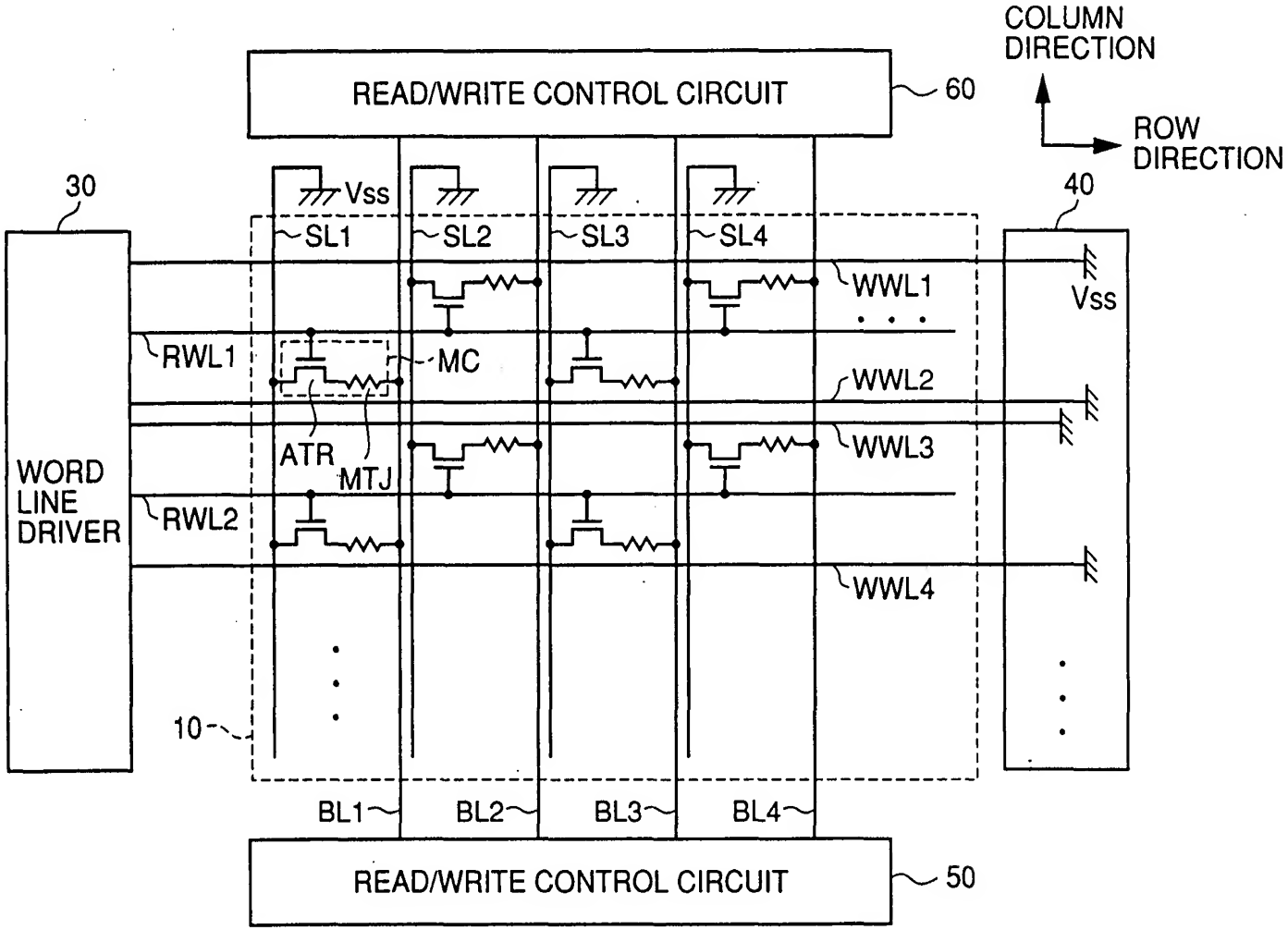
COLUMN DIRECTION
ROW DIRECTION
READ/WRITE CONTROL CIRCUIT
60
30
40
Vss
SL1
SL2
SL3
SL4
WWL1
Vss
RWL1
MC
WWL2
ATR
MTJ
WWL3
WORD LINE DRIVER
RWL2
WWL4
10
BL1
BL2
BL3
BL4
READ/WRITE CONTROL CIRCUIT
50

FIG.10

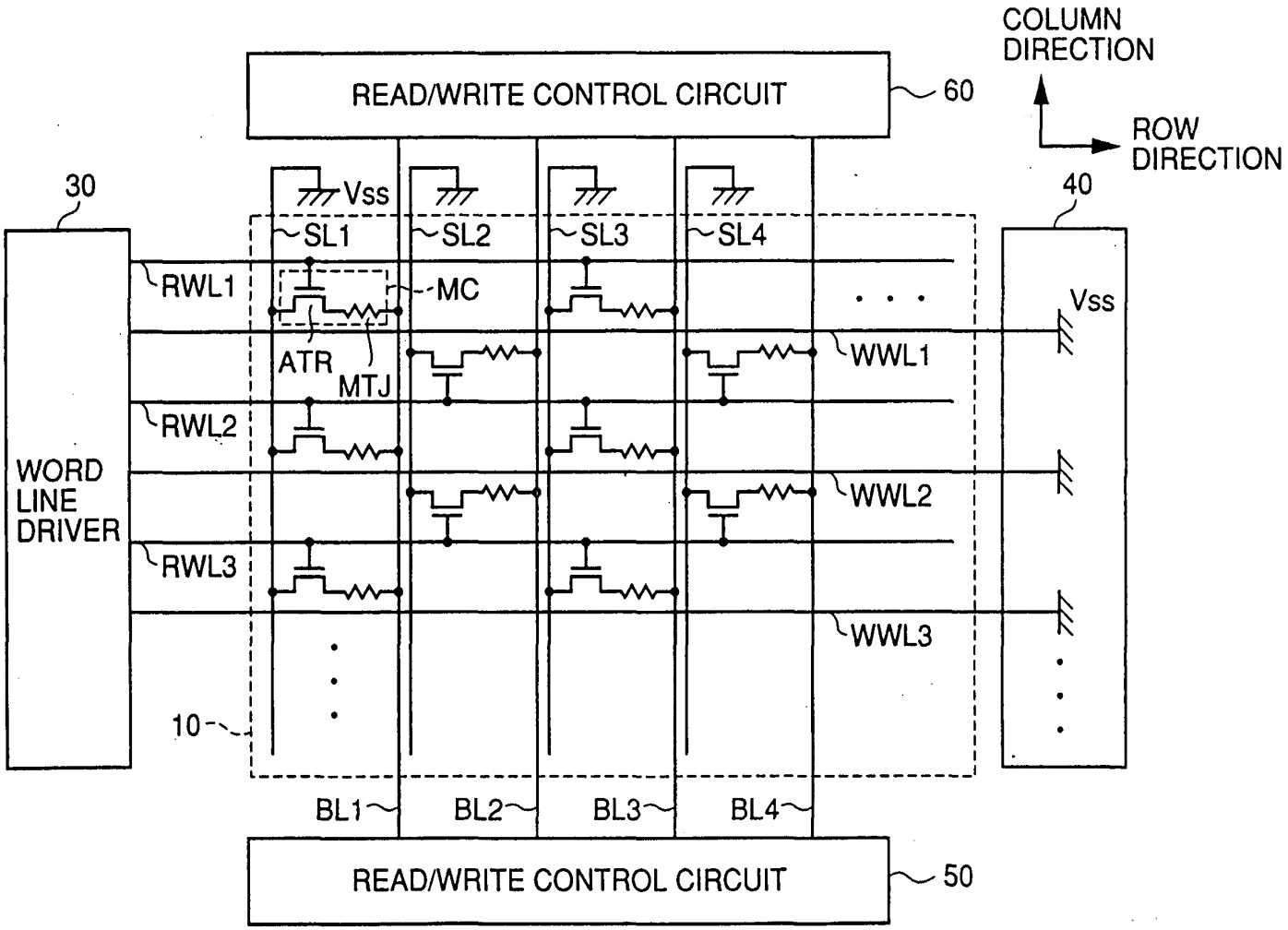
COLUMN DIRECTION
ROW DIRECTION
READ/WRITE CONTROL CIRCUIT
60
30
40
Vss
SL1
SL2
SL3
SL4
RWL1
MC
ATR
MTJ
WWL1
RWL2
WWL2
WORD LINE DRIVER
RWL3
WWL3
10
BL1
BL2
BL3
BL4
READ/WRITE CONTROL CIRCUIT
50

FIG.11

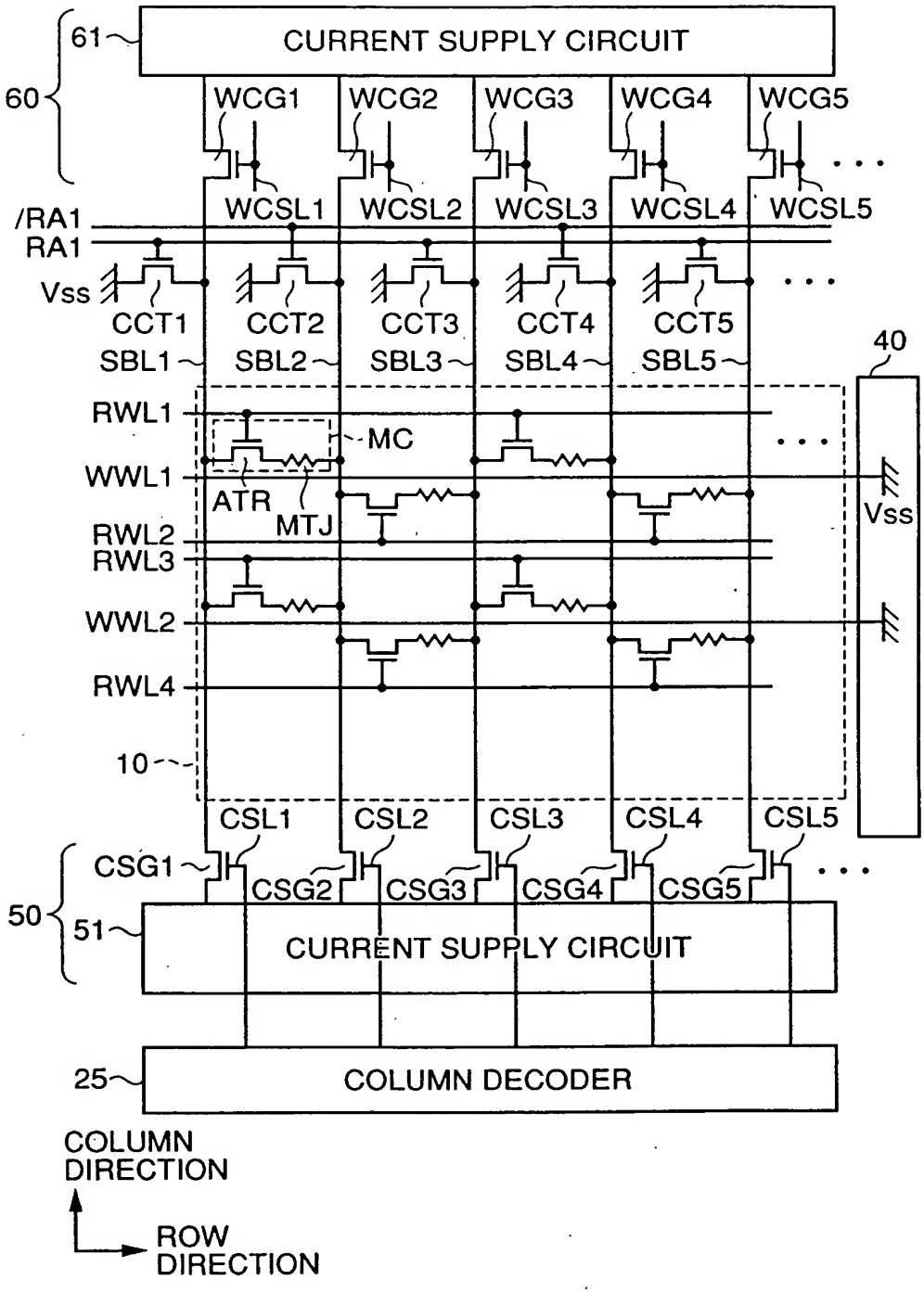
61
CURRENT SUPPLY CIRCUIT
60
WCG1
WCG2
WCG3
WCG4
WCG5
WCSL1
WCSL2
WCSL3
WCSL4
WCSL5
/RA1
RA1
Vss
CCT1
CCT2
CCT3
CCT4
CCT5
SBL1
SBL2
SBL3
SBL4
SBL5
40
RWL1
MC
WWL1
ATR
MTJ
Vss
RWL2
RWL3
WWL2
RWL4
10
CSL1
CSL2
CSL3
CSL4
CSL5
CSG1
CSG2
CSG3
CSG4
CSG5
50
51
CURRENT SUPPLY CIRCUIT
25
COLUMN DECODER
COLUMN DIRECTION
ROW DIRECTION

FIG.12

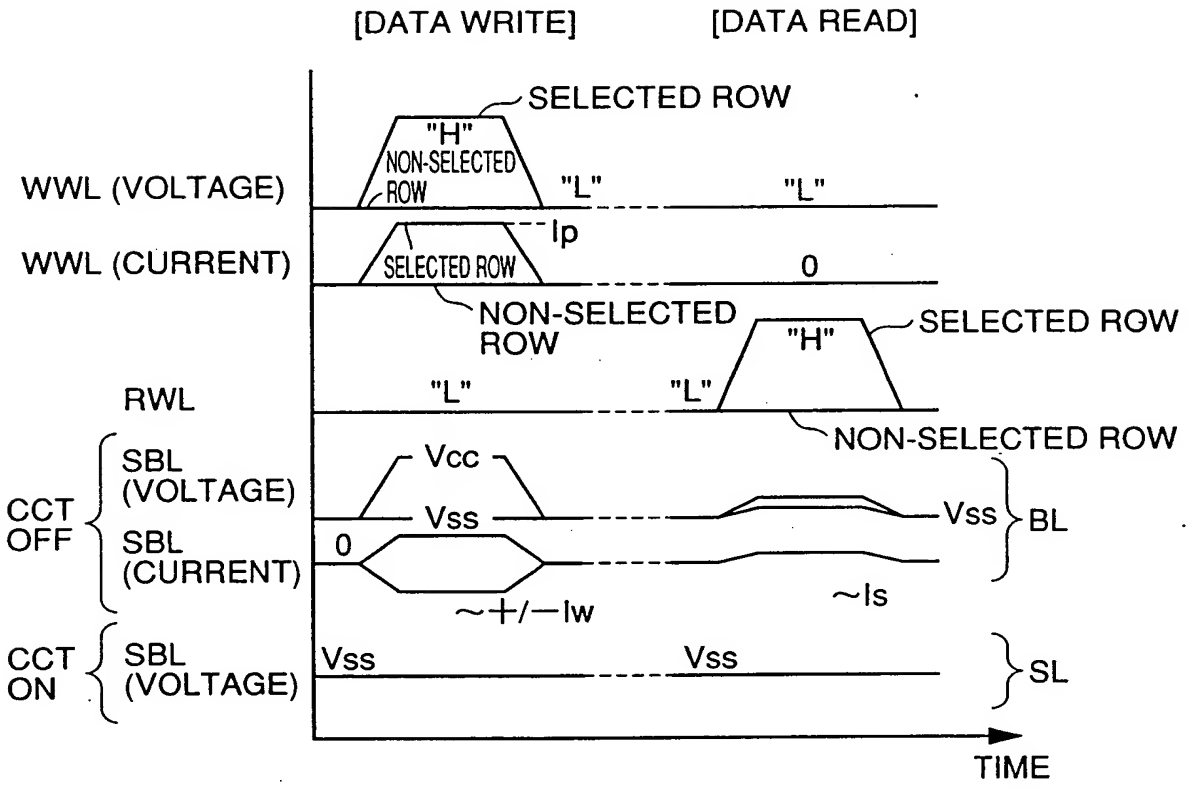
[DATA WRITE]
[DATA READ]
SELECTED ROW
"H"
NON-SELECTED ROW
WWL (VOLTAGE)
"L"
"L"
Ip
WWL (CURRENT)
SELECTED ROW
0
NON-SELECTED ROW
"H"
SELECTED ROW
RWL
"L"
"L"
NON-SELECTED ROW
Vcc
SBL (VOLTAGE)
CCT OFF
Vss
Vss
BL
0
SBL (CURRENT)
~+/−Iw
~Is
CCT ON
SBL (VOLTAGE)
Vss
Vss
SL
TIME

FIG.13

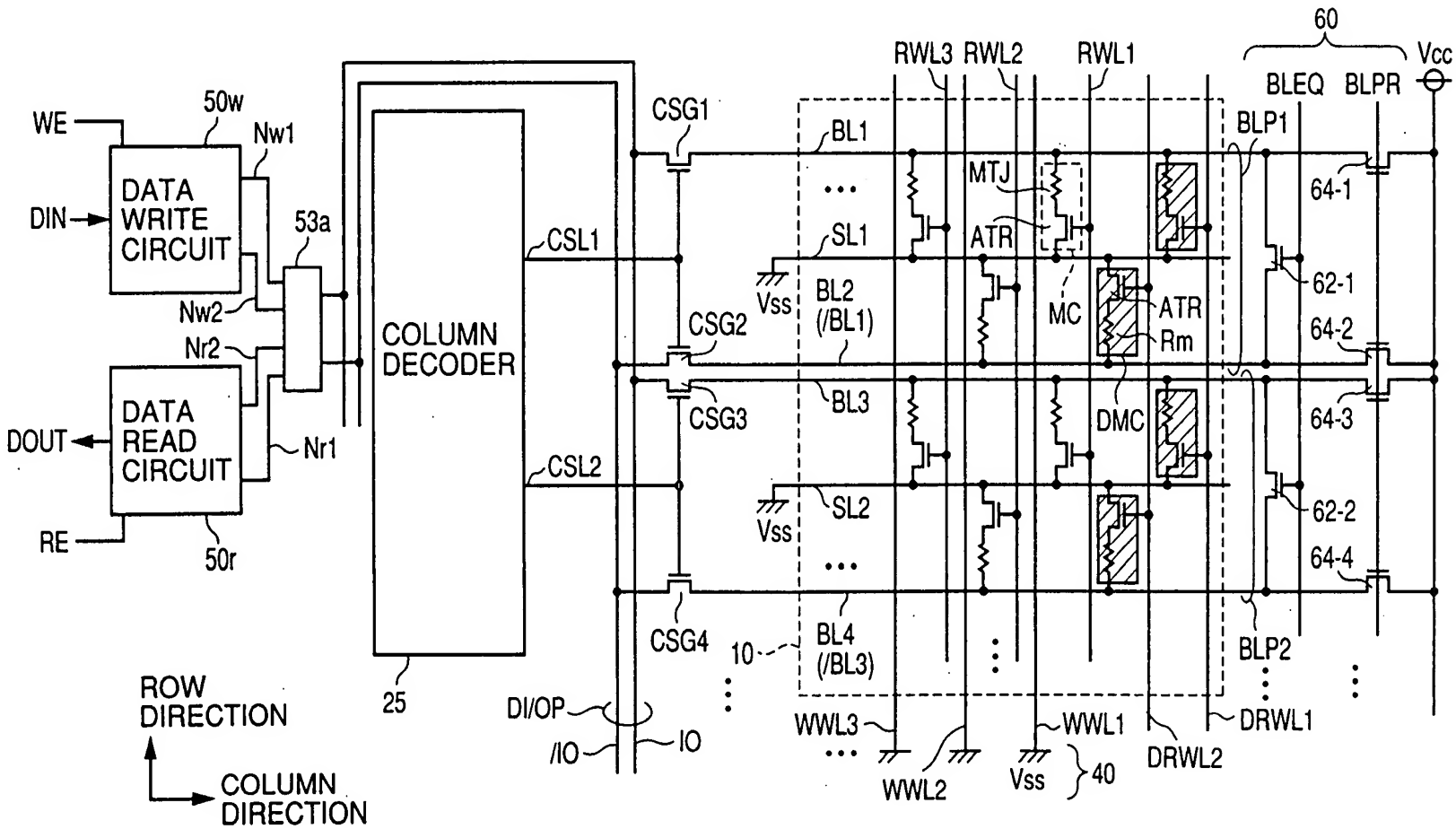
WE
50w
Nw1
DIN
DATA WRITE CIRCUIT
53a
Nw2
Nr2
DATA READ CIRCUIT
DOUT
Nr1
RE
50r
COLUMN DECODER
25
CSL1
CSL2
CSG1
CSG2
CSG3
CSG4
BL1
SL1
BL2 (/BL1)
BL3
SL2
BL4 (/BL3)
10
Vss
RWL3
RWL2
RWL1
MTJ
ATR
MC
Rm
DMC
60
BLEQ
BLPR
Vcc
BLP1
BLP2
64-1
62-1
64-2
64-3
62-2
64-4
DRWL1
DRWL2
WWL3
WWL2
WWL1
40
DI/OP
/IO
IO
ROW DIRECTION
COLUMN DIRECTION

FIG.14

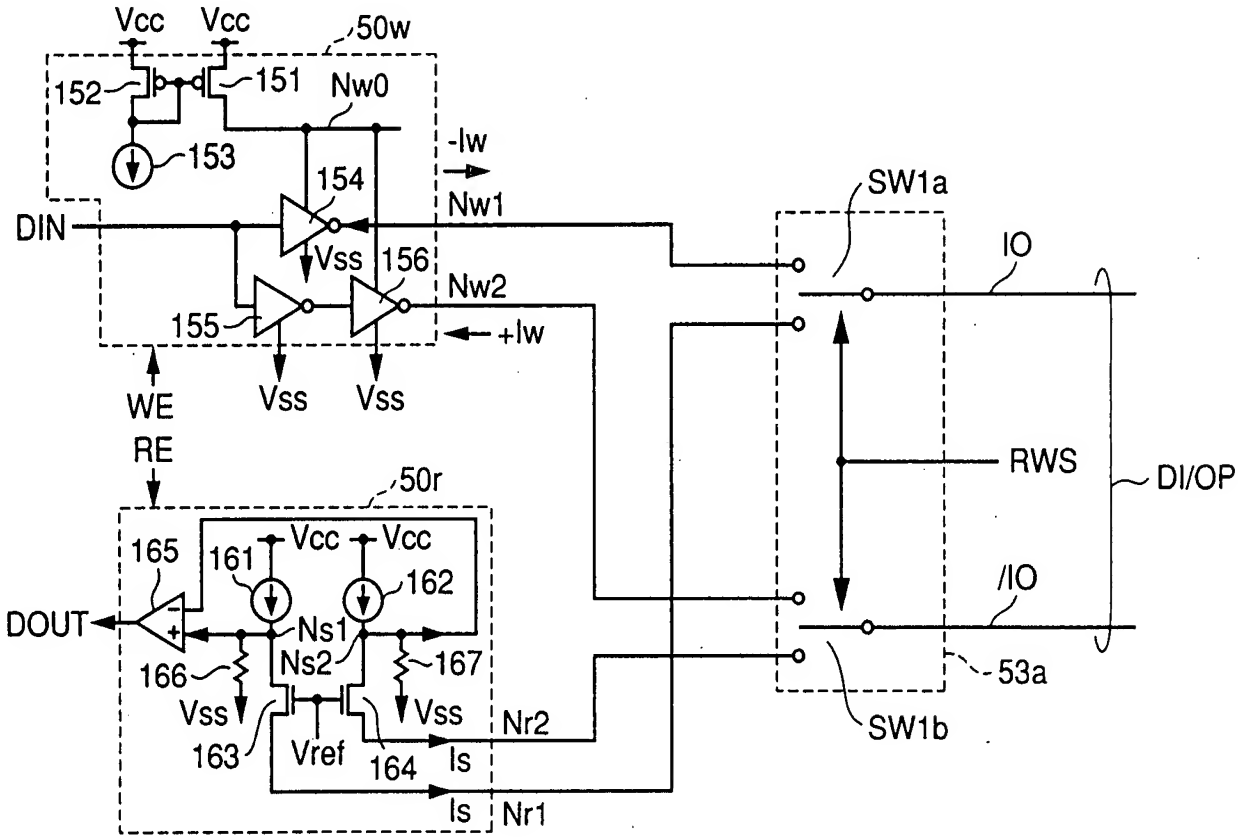
Vcc
Vcc
50w
152
151
Nw0
153
-Iw
154
Nw1
DIN
Vss
156
Nw2
155
+Iw
WE
Vss
Vss
RE
50r
165
161
Vcc
Vcc
162
DOUT
Ns1
Ns2
166
167
Vss
Vss
Nr2
163
Vref
164
Is
Is
Nr1
SW1a
IO
RWS
DI/OP
/IO
53a
SW1b

FIG.15

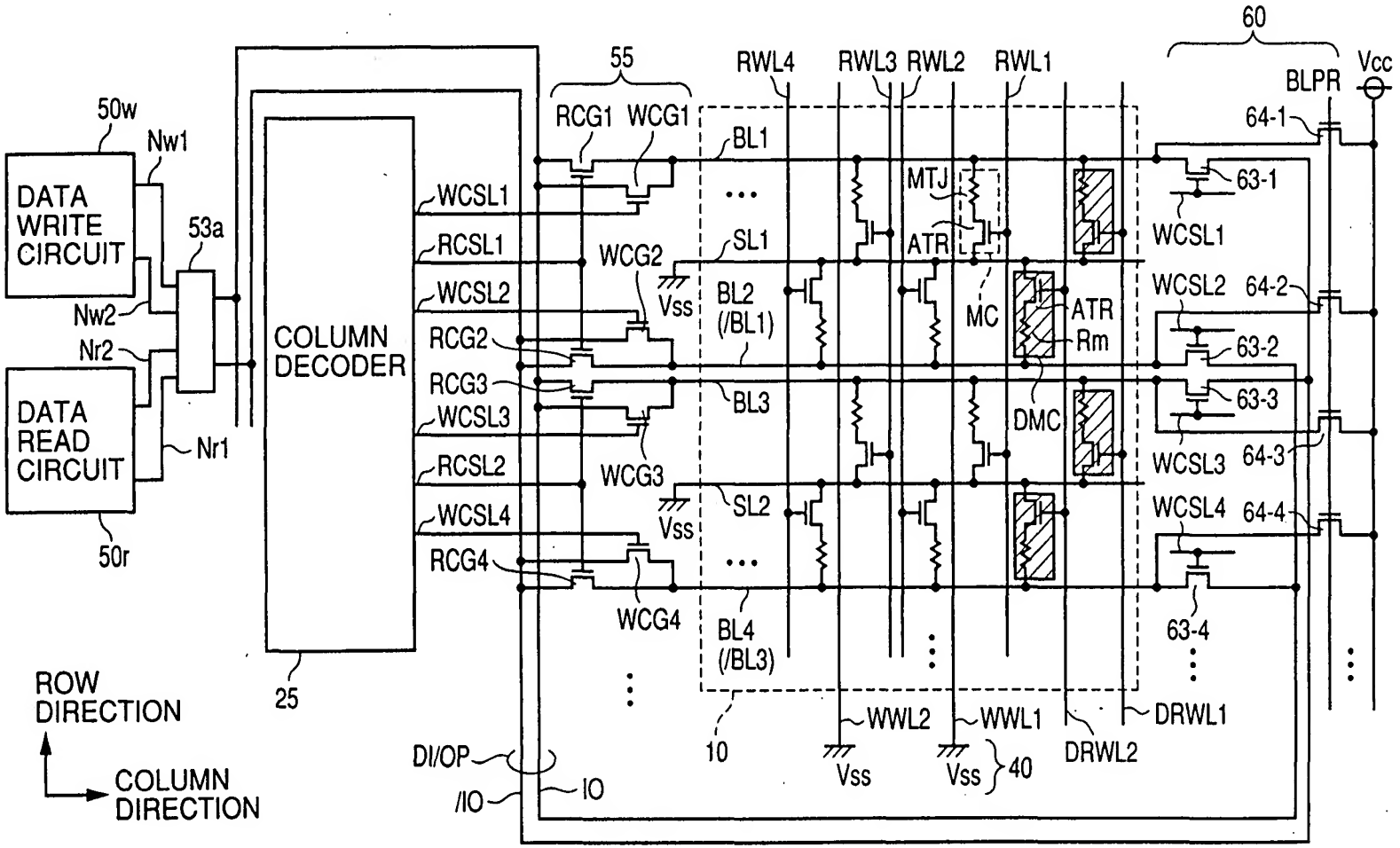
50w
Nw1
DATA WRITE CIRCUIT
53a
Nw2
Nr2
DATA READ CIRCUIT
Nr1
50r
COLUMN DECODER
25
55
RCG1
WCG1
WCSL1
RCSL1
WCSL2
RCG2
RCG3
WCSL3
RCSL2
WCSL4
RCG4
WCG2
WCG3
WCG4
Vss
RWL4
RWL3
RWL2
RWL1
BL1
SL1
BL2 (/BL1)
BL3
SL2
BL4 (/BL3)
MTJ
ATR
MC
DMC
Rm
60
BLPR
Vcc
64-1
63-1
64-2
63-2
63-3
64-3
WCSL4
64-4
63-4
DRWL1
DRWL2
WWL2
WWL1
10
40
DI/OP
/IO
IO
ROW DIRECTION
COLUMN DIRECTION

FIG.16

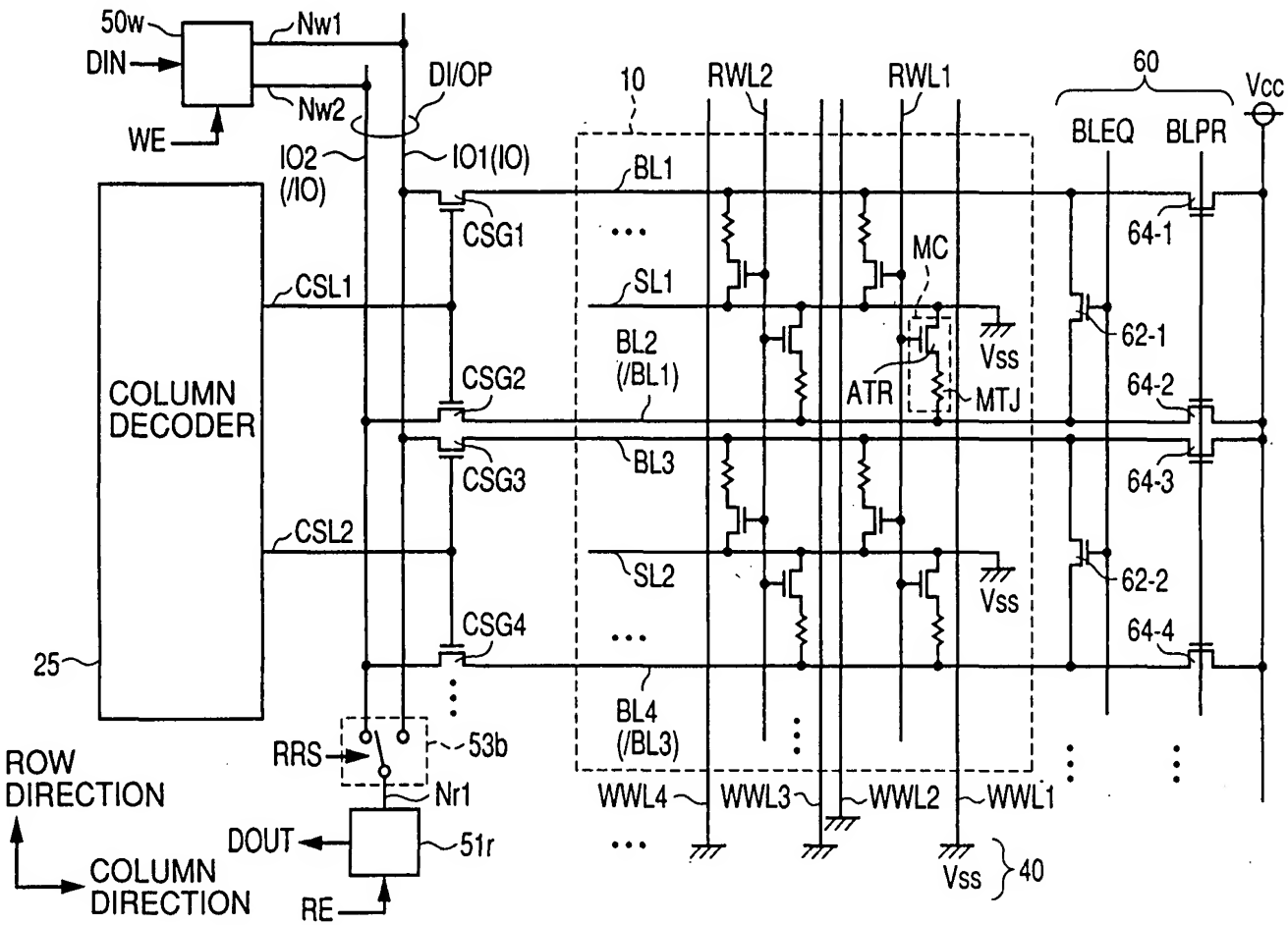
50w
DIN
WE
Nw1
Nw2
DI/OP
IO2
(/IO)
IO1(IO)
10
RWL2
RWL1
60
Vcc
BLEQ
BLPR
BL1
CSG1
SL1
MC
64-1
CSL1
62-1
BL2
(/BL1)
CSG2
ATR
MTJ
Vss
64-2
COLUMN
DECODER
BL3
CSG3
64-3
CSL2
SL2
62-2
CSG4
64-4
25
BL4
(/BL3)
RRS
53b
Nr1
ROW
DIRECTION
WWL4
WWL3
WWL2
WWL1
DOUT
51r
COLUMN
DIRECTION
RE
Vss
40

FIG. 17

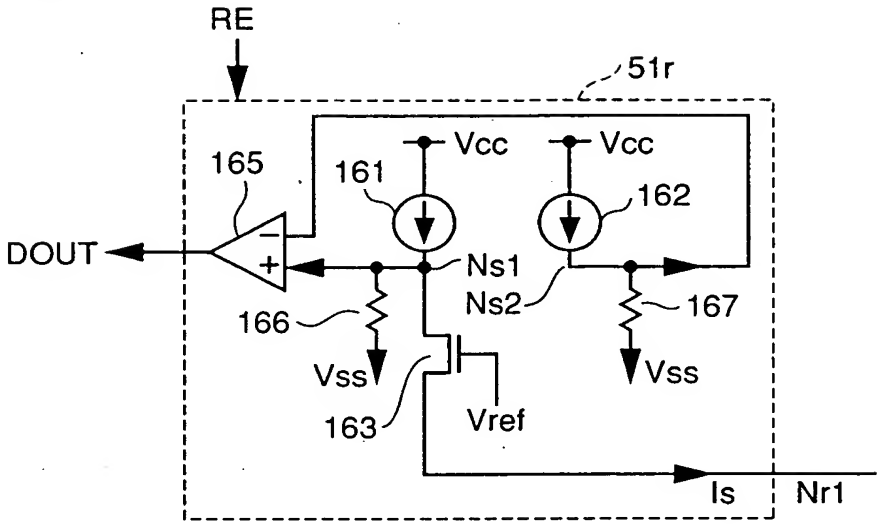

FIG. 18

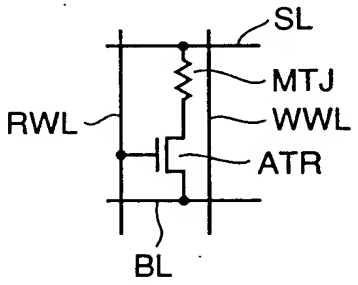

FIG. 19

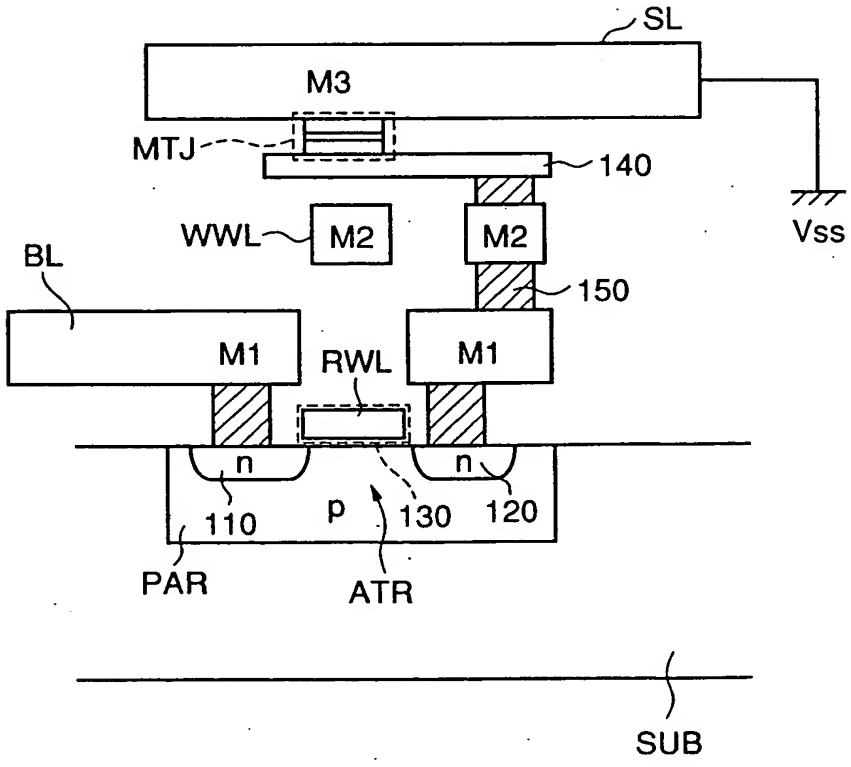

FIG.20

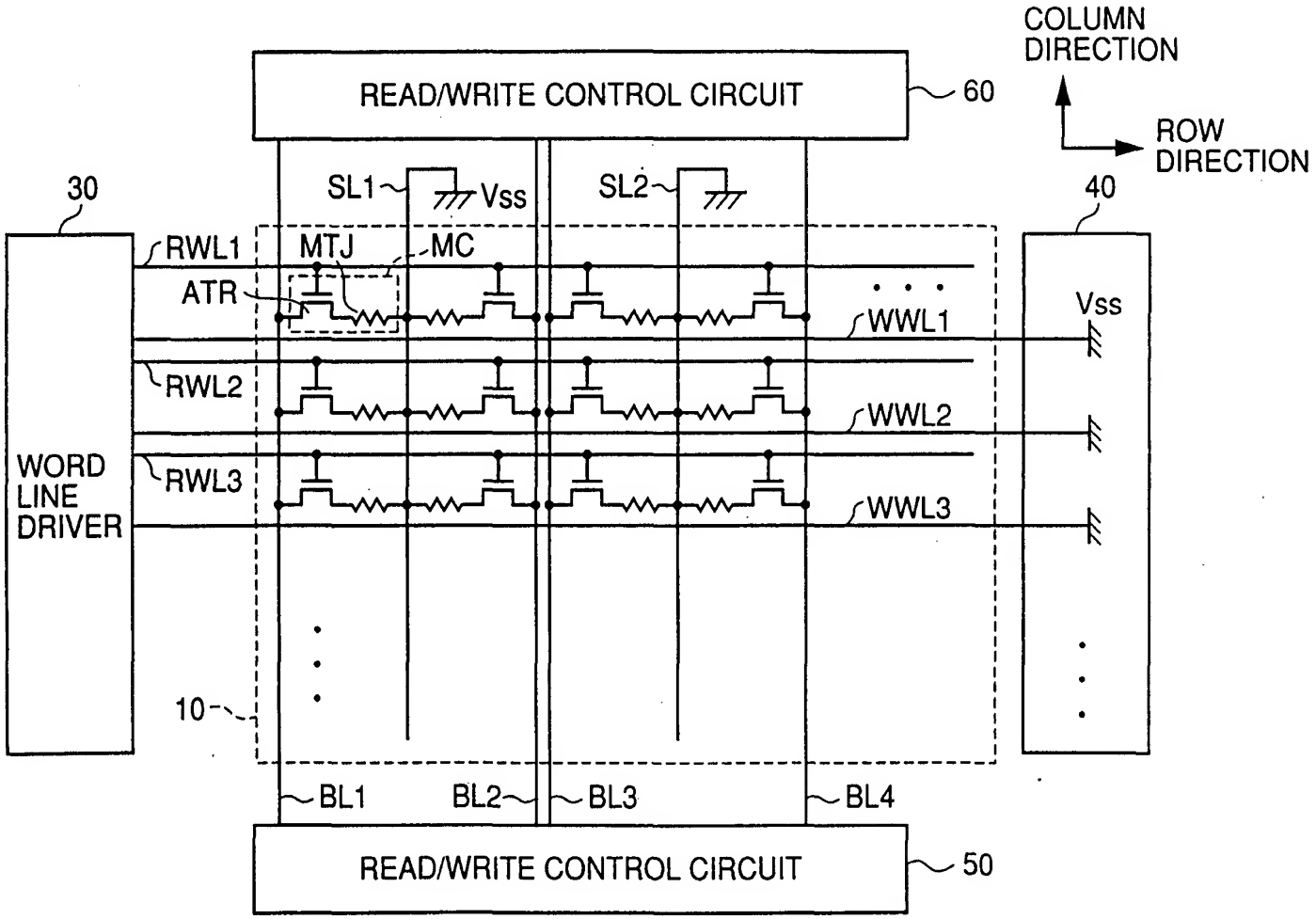
COLUMN DIRECTION
ROW DIRECTION
READ/WRITE CONTROL CIRCUIT
60
30
40
SL1
Vss
SL2
RWL1
MTJ
MC
ATR
WWL1
Vss
RWL2
WWL2
WORD LINE DRIVER
RWL3
WWL3
10
BL1
BL2
BL3
BL4
READ/WRITE CONTROL CIRCUIT
50

FIG.21

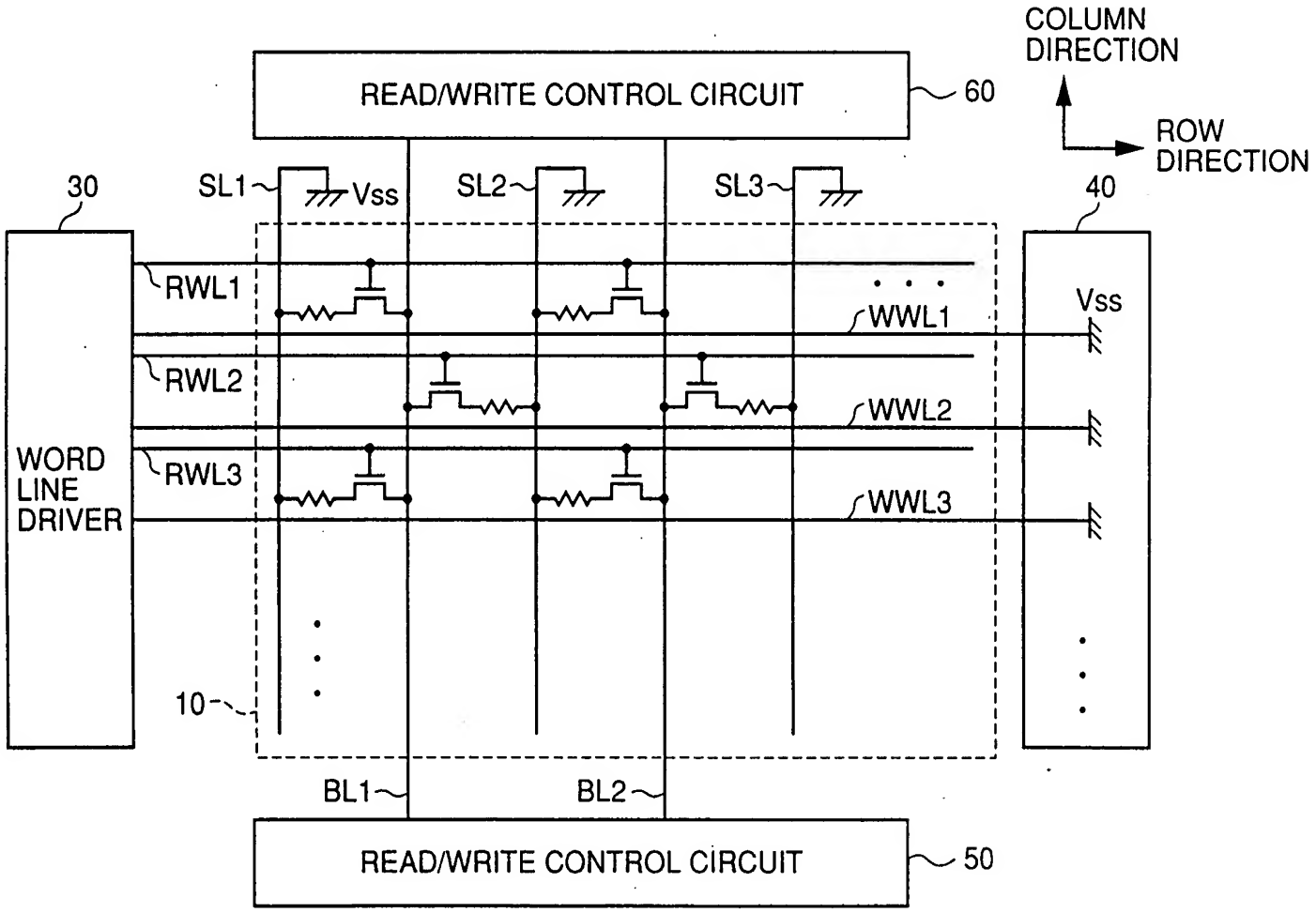
COLUMN DIRECTION
ROW DIRECTION
READ/WRITE CONTROL CIRCUIT
60
30
SL1
Vss
SL2
SL3
40
RWL1
WWL1
Vss
RWL2
WWL2
WORD LINE DRIVER
RWL3
WWL3
10
BL1
BL2
READ/WRITE CONTROL CIRCUIT
50

FIG.22

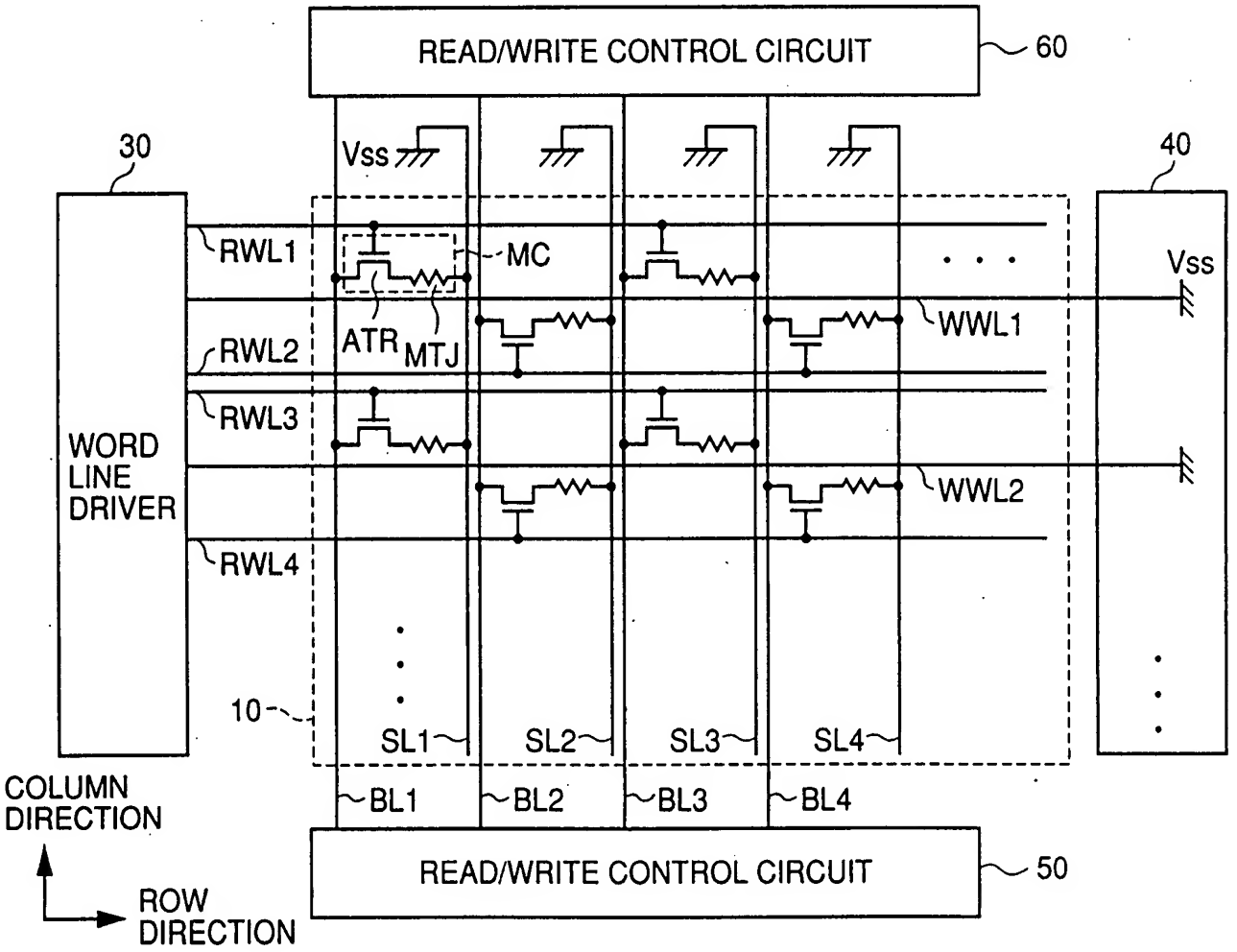
READ/WRITE CONTROL CIRCUIT
60
30
40
Vss
RWL1
MC
RWL2
ATR
MTJ
WWL1
RWL3
WORD LINE DRIVER
WWL2
RWL4
10
SL1
SL2
SL3
SL4
BL1
BL2
BL3
BL4
COLUMN DIRECTION
ROW DIRECTION
READ/WRITE CONTROL CIRCUIT
50

FIG.23

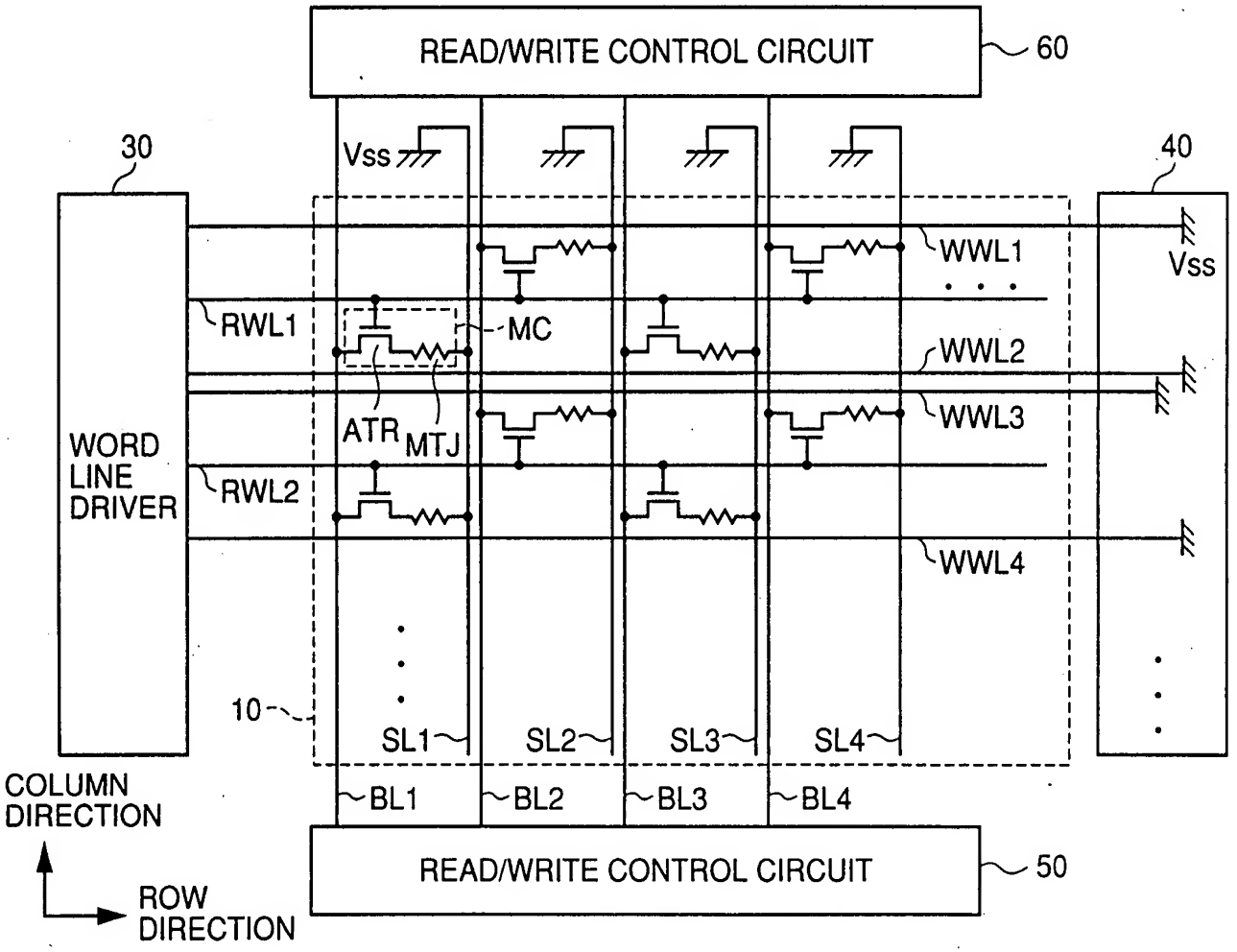
READ/WRITE CONTROL CIRCUIT
60
30
40
Vss
WWL1
Vss
RWL1
MC
WWL2
ATR
MTJ
WWL3
WORD LINE DRIVER
RWL2
WWL4
10
SL1
SL2
SL3
SL4
BL1
BL2
BL3
BL4
COLUMN DIRECTION
ROW DIRECTION
READ/WRITE CONTROL CIRCUIT
50

FIG.24

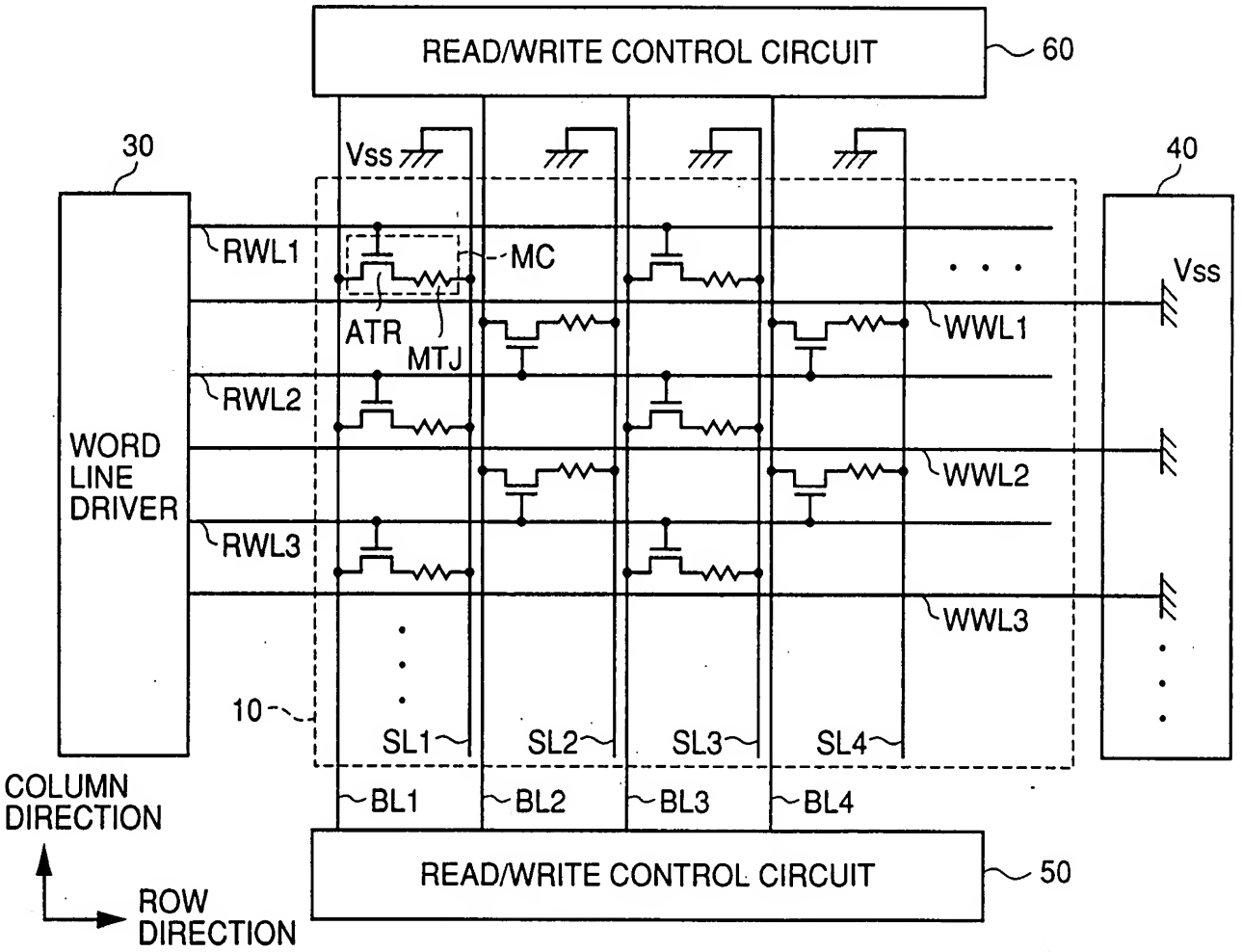
READ/WRITE CONTROL CIRCUIT
60
30
40
Vss
RWL1
MC
ATR
MTJ
WWL1
RWL2
WWL2
WORD
LINE
DRIVER
RWL3
WWL3
10
SL1
SL2
SL3
SL4
BL1
BL2
BL3
BL4
READ/WRITE CONTROL CIRCUIT
50
COLUMN
DIRECTION
ROW
DIRECTION

FIG.25

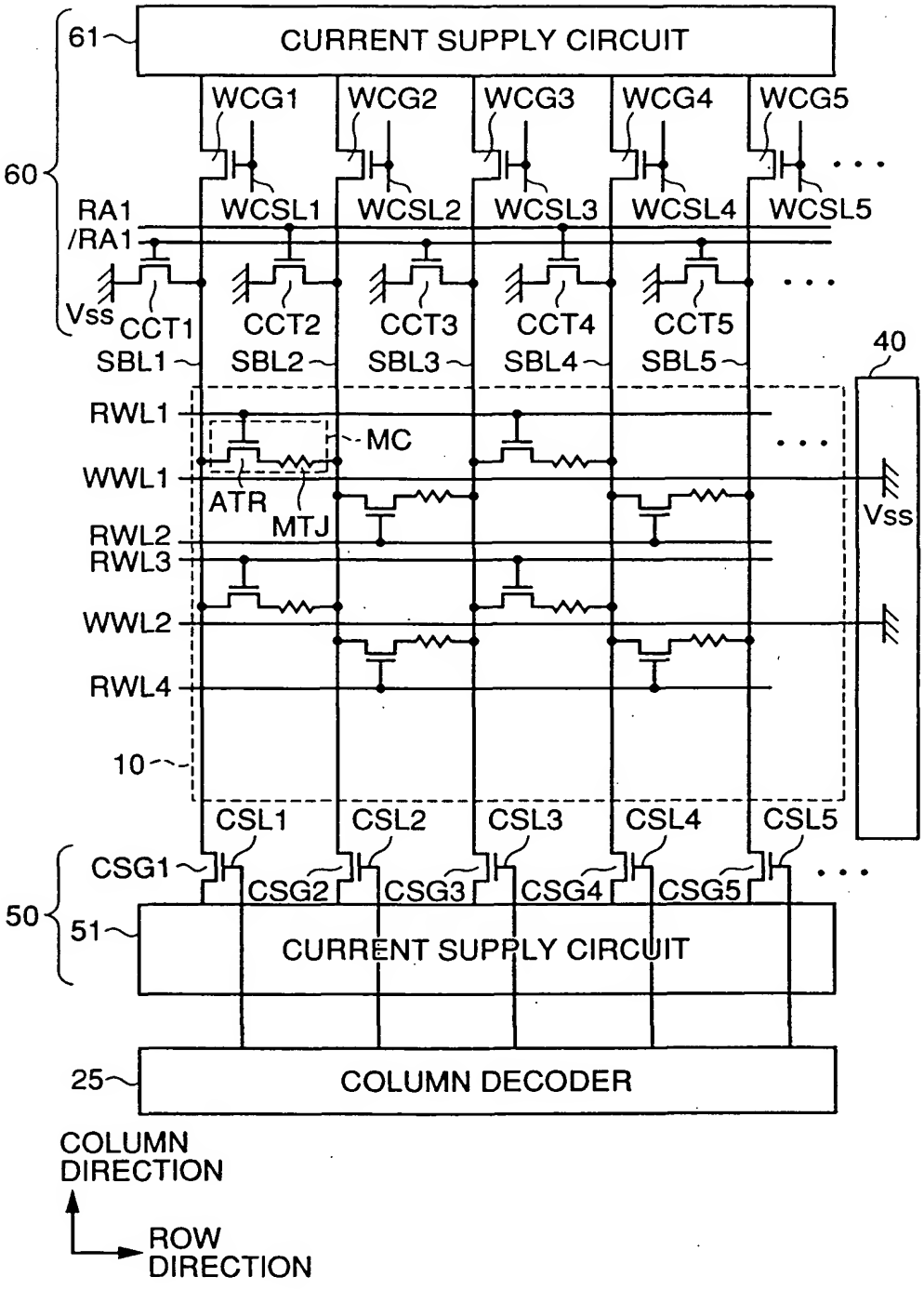
61
CURRENT SUPPLY CIRCUIT
WCG1
WCG2
WCG3
WCG4
WCG5
60
RA1
/RA1
WCSL1
WCSL2
WCSL3
WCSL4
WCSL5
Vss
CCT1
CCT2
CCT3
CCT4
CCT5
SBL1
SBL2
SBL3
SBL4
SBL5
40
RWL1
MC
WWL1
ATR
MTJ
Vss
RWL2
RWL3
WWL2
RWL4
10
CSL1
CSL2
CSL3
CSL4
CSL5
CSG1
CSG2
CSG3
CSG4
CSG5
50
51
CURRENT SUPPLY CIRCUIT
25
COLUMN DECODER
COLUMN DIRECTION
ROW DIRECTION

FIG.26

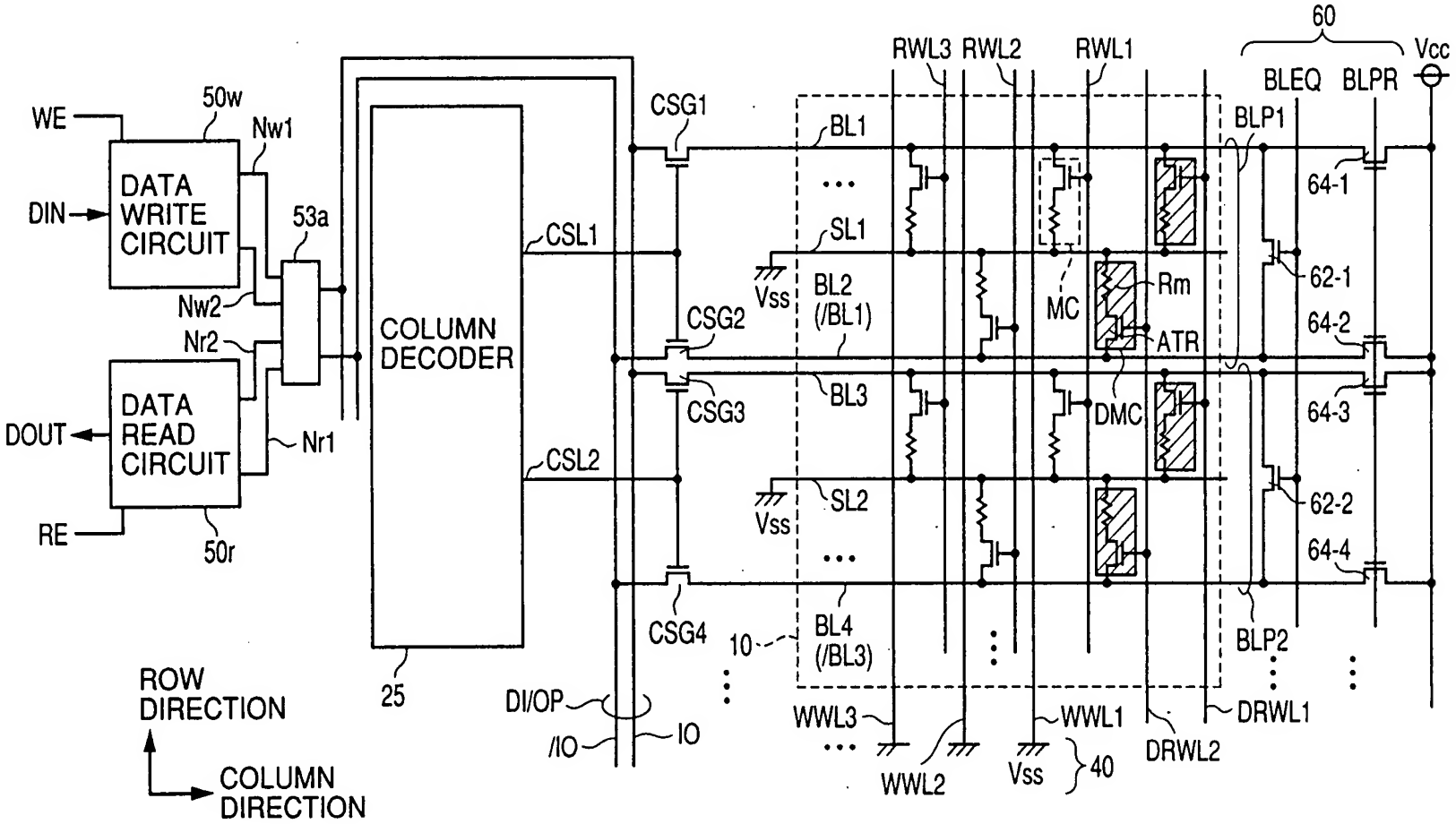
WE
DIN
DOUT
RE
50w
Nw1
Nw2
Nr2
53a
Nr1
50r
DATA WRITE CIRCUIT
DATA READ CIRCUIT
COLUMN DECODER
25
CSL1
CSL2
CSG1
CSG2
CSG3
CSG4
BL1
SL1
BL2 (/BL1)
SL2
BL3
BL4 (/BL3)
10
Vss
RWL3
RWL2
RWL1
MC
Rm
ATR
DMC
60
BLEQ
BLPR
Vcc
BLP1
BLP2
64-1
62-1
64-2
64-3
62-2
64-4
DRWL1
DRWL2
WWL3
WWL2
WWL1
Vss
40
DI/OP
/IO
IO
ROW DIRECTION
COLUMN DIRECTION

FIG.27

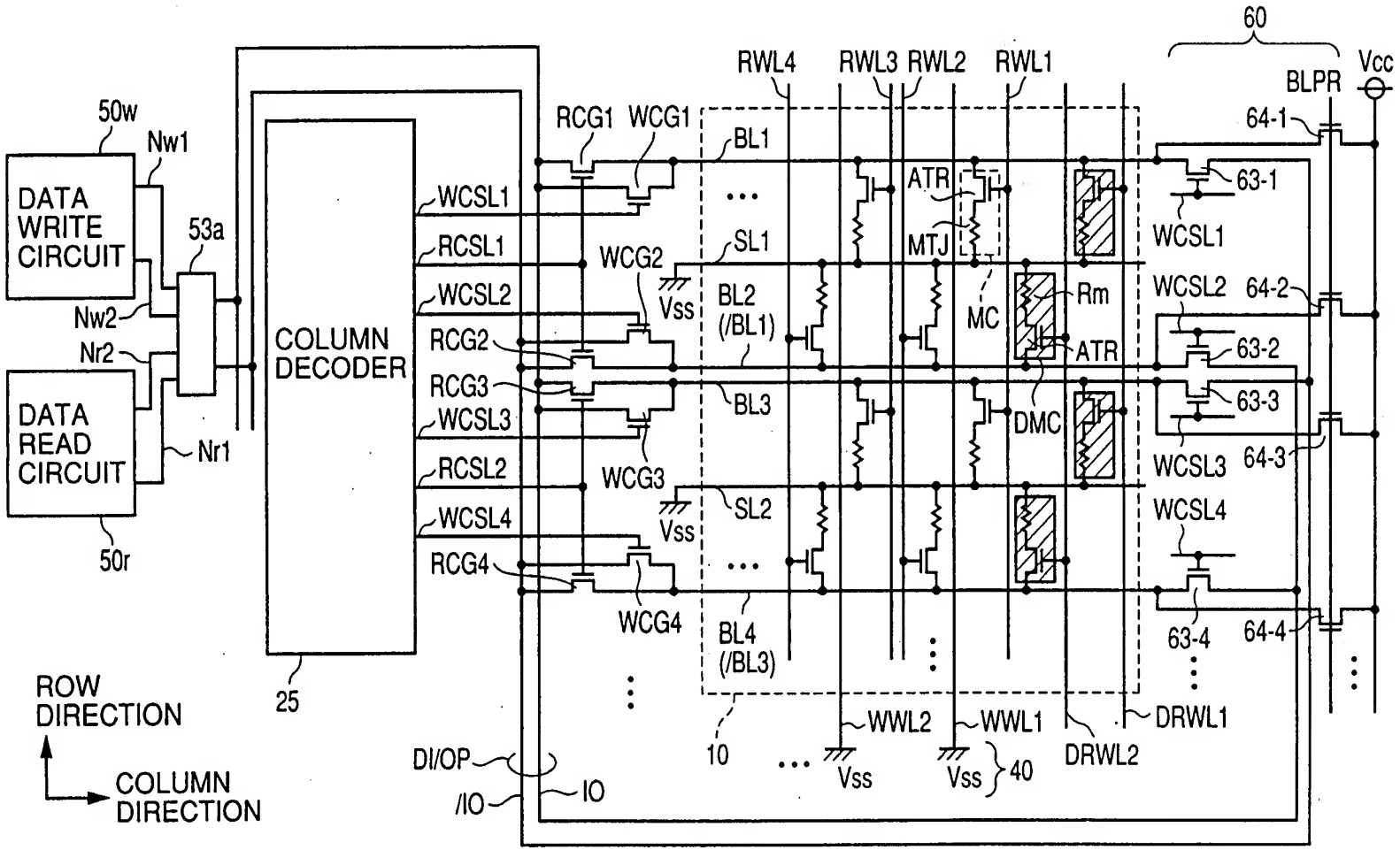
50w
Nw1
DATA WRITE CIRCUIT
53a
Nw2
Nr2
DATA READ CIRCUIT
Nr1
50r
COLUMN DECODER
25
WCSL1
RCSL1
WCSL2
RCG2
RCG3
WCSL3
RCSL2
WCSL4
RCG4
RCG1
WCG1
WCG2
WCG3
WCG4
Vss
BL1
SL1
BL2 (/BL1)
BL3
SL2
BL4 (/BL3)
10
RWL4
RWL3
RWL2
RWL1
ATR
MTJ
MC
Rm
DMC
WWL2
WWL1
Vss
Vss
40
DRWL2
DRWL1
60
BLPR
Vcc
64-1
63-1
WCSL1
WCSL2
64-2
63-2
63-3
WCSL3
64-3
WCSL4
63-4
64-4
DI/OP
/IO
IO
ROW DIRECTION
COLUMN DIRECTION

FIG.28

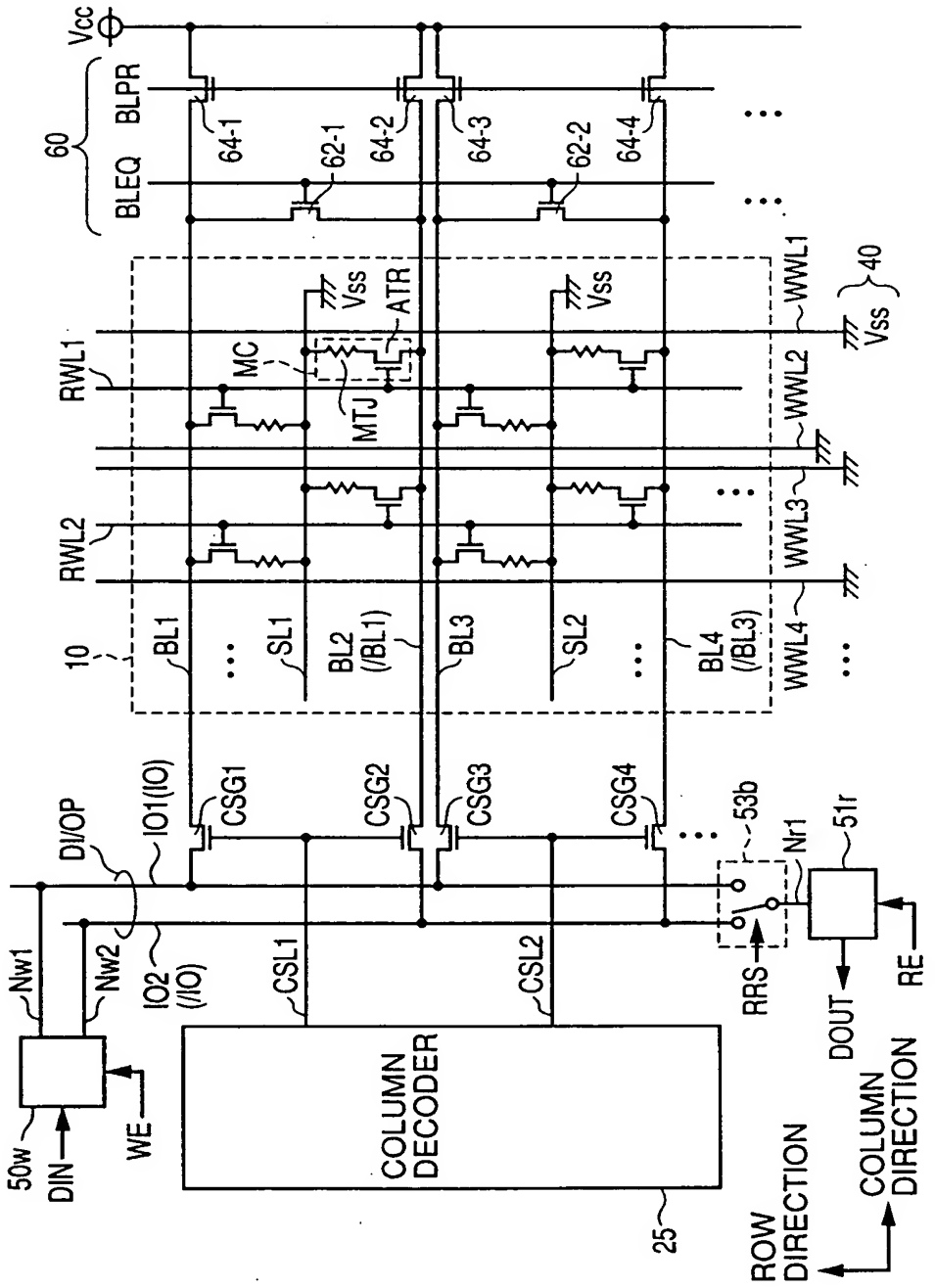
Vcc
60
BLPR
BLEQ
64-1
62-1
64-2
64-3
62-2
64-4
RWL1
RWL2
MC
MTJ
ATR
Vss
WWL1
WWL2
WWL3
WWL4
40
10
BL1
SL1
BL2 (/BL1)
BL3
SL2
BL4 (/BL3)
DI/OP
IO1(IO)
IO2 (/IO)
CSG1
CSG2
CSG3
CSG4
CSL1
CSL2
53b
Nr1
51r
Nw1
Nw2
50w
DIN
WE
RRS
DOUT
RE
COLUMN DECODER
25
ROW DIRECTION
COLUMN DIRECTION

FIG.29

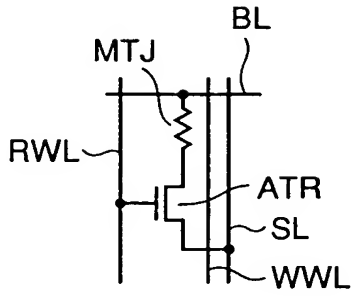
BL
MTJ
RWL
ATR
SL
WWL

FIG.30

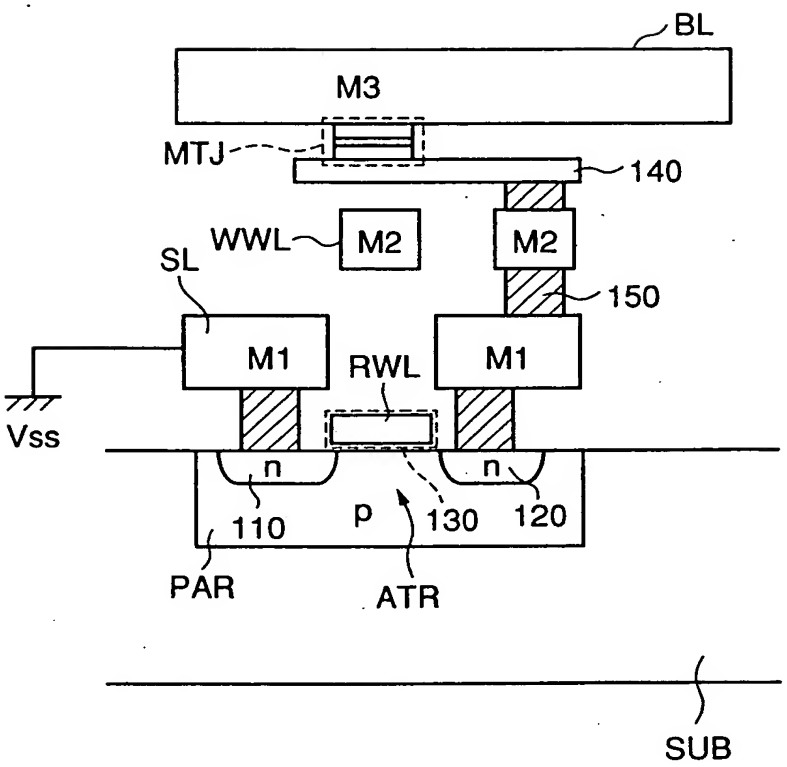
BL
M3
MTJ
140
WWL
M2
M2
SL
150
M1
RWL
M1
Vss
n
n
110
p
130
120
PAR
ATR
SUB

FIG.31

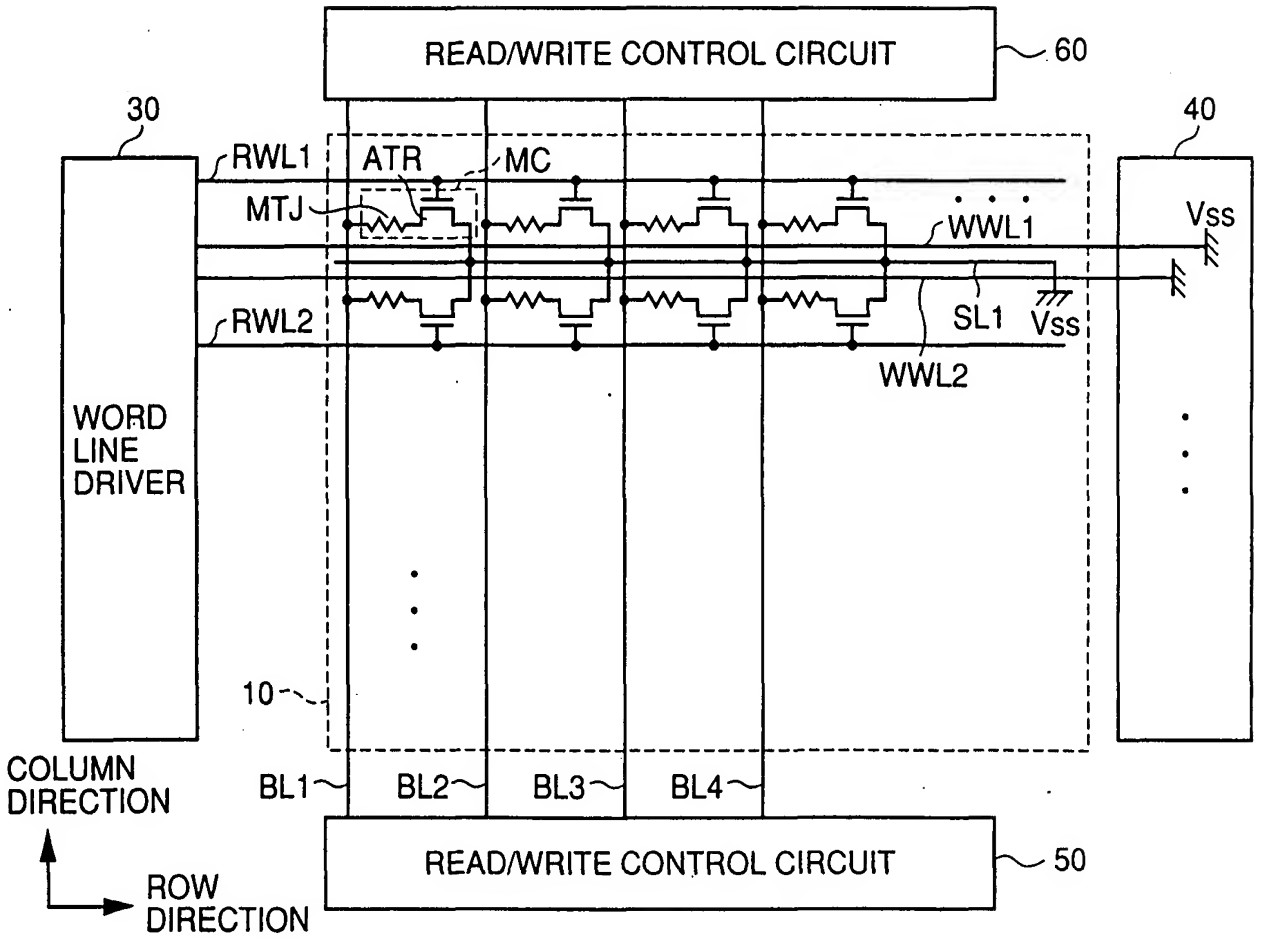
READ/WRITE CONTROL CIRCUIT
60
30
40
RWL1
ATR
MC
MTJ
WWL1
Vss
RWL2
SL1
Vss
WWL2
WORD
LINE
DRIVER
10
COLUMN
DIRECTION
BL1
BL2
BL3
BL4
READ/WRITE CONTROL CIRCUIT
50
ROW
DIRECTION

FIG.32

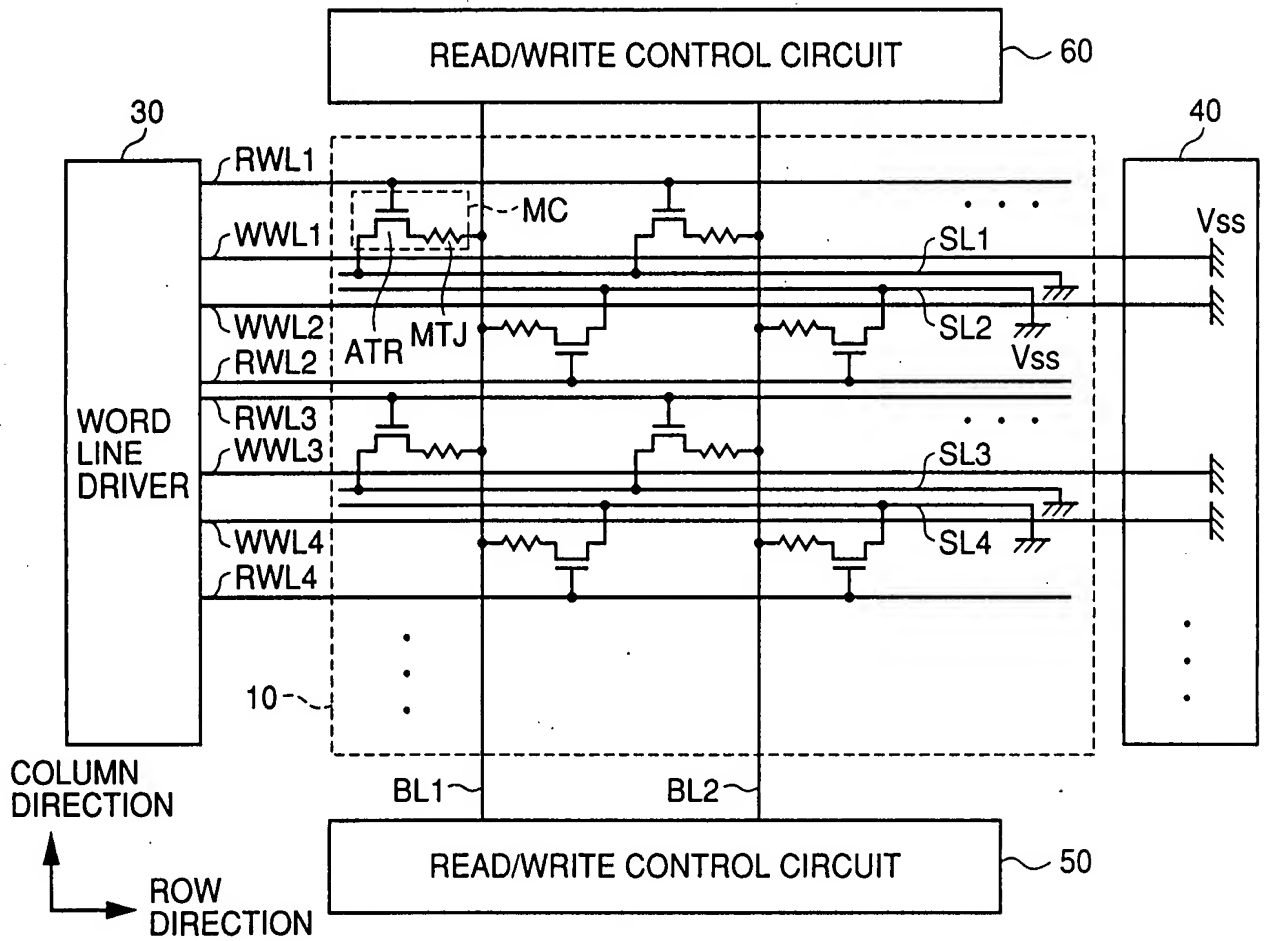
READ/WRITE CONTROL CIRCUIT
60
30
40
RWL1
WWL1
MC
SL1
Vss
WWL2
RWL2
ATR
MTJ
SL2
Vss
WORD LINE DRIVER
RWL3
WWL3
SL3
WWL4
RWL4
SL4
10
BL1
BL2
COLUMN DIRECTION
ROW DIRECTION
READ/WRITE CONTROL CIRCUIT
50

FIG.33

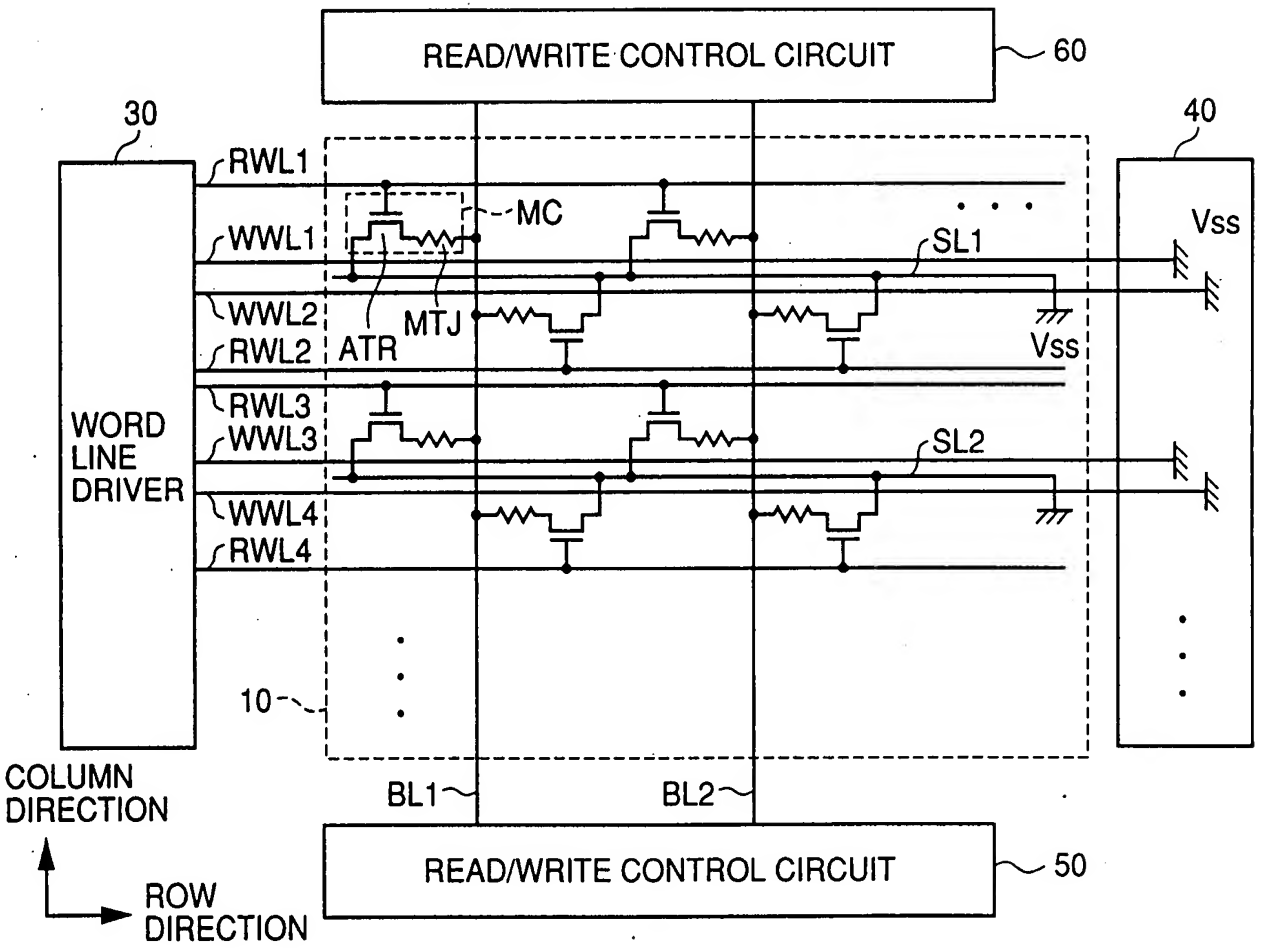
READ/WRITE CONTROL CIRCUIT
60
30
40
RWL1
WWL1
WWL2
RWL2
RWL3
WWL3
WWL4
RWL4
MC
MTJ
ATR
SL1
SL2
Vss
Vss
WORD LINE DRIVER
10
BL1
BL2
COLUMN DIRECTION
ROW DIRECTION
READ/WRITE CONTROL CIRCUIT
50

FIG.34

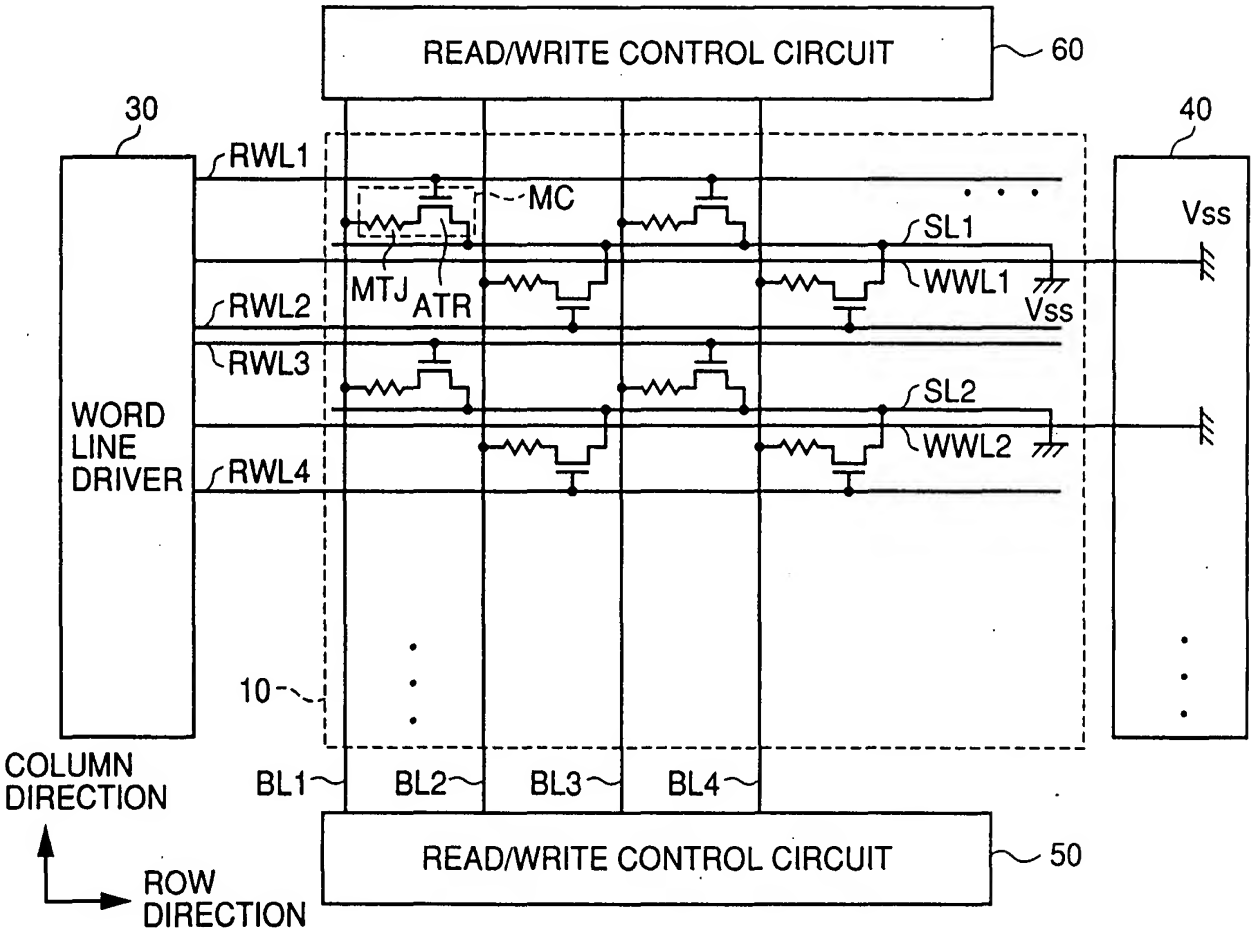
READ/WRITE CONTROL CIRCUIT
60
30
40
RWL1
MC
SL1
Vss
MTJ
ATR
WWL1
RWL2
Vss
RWL3
SL2
WORD
LINE
DRIVER
WWL2
RWL4
10
COLUMN
DIRECTION
BL1
BL2
BL3
BL4
READ/WRITE CONTROL CIRCUIT
50
ROW
DIRECTION

FIG.35

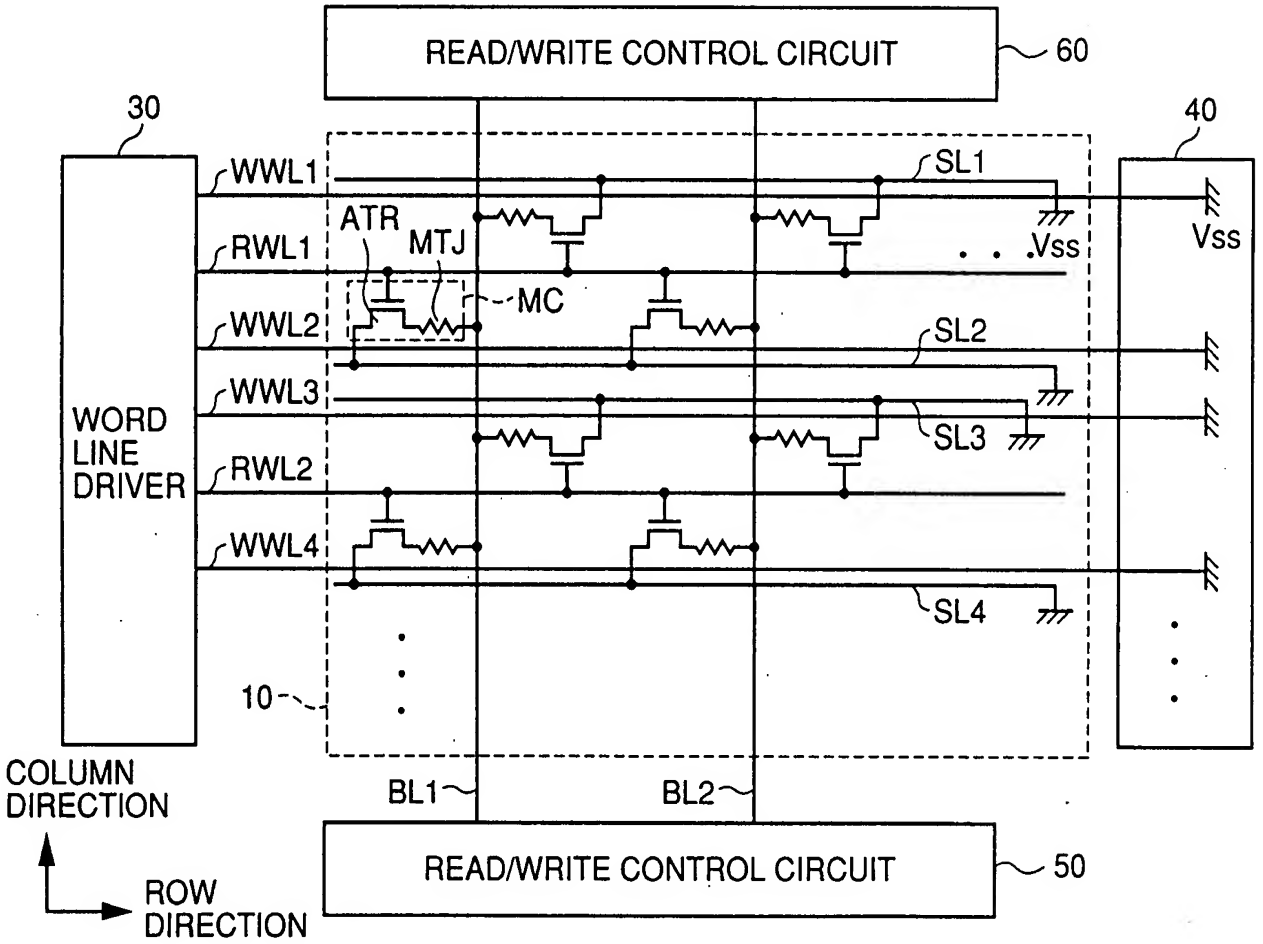
READ/WRITE CONTROL CIRCUIT
60
30
40
WWL1
SL1
ATR
MTJ
RWL1
Vss
Vss
MC
WWL2
SL2
WWL3
SL3
WORD LINE DRIVER
RWL2
WWL4
SL4
10
BL1
BL2
COLUMN DIRECTION
ROW DIRECTION
READ/WRITE CONTROL CIRCUIT
50

FIG.36

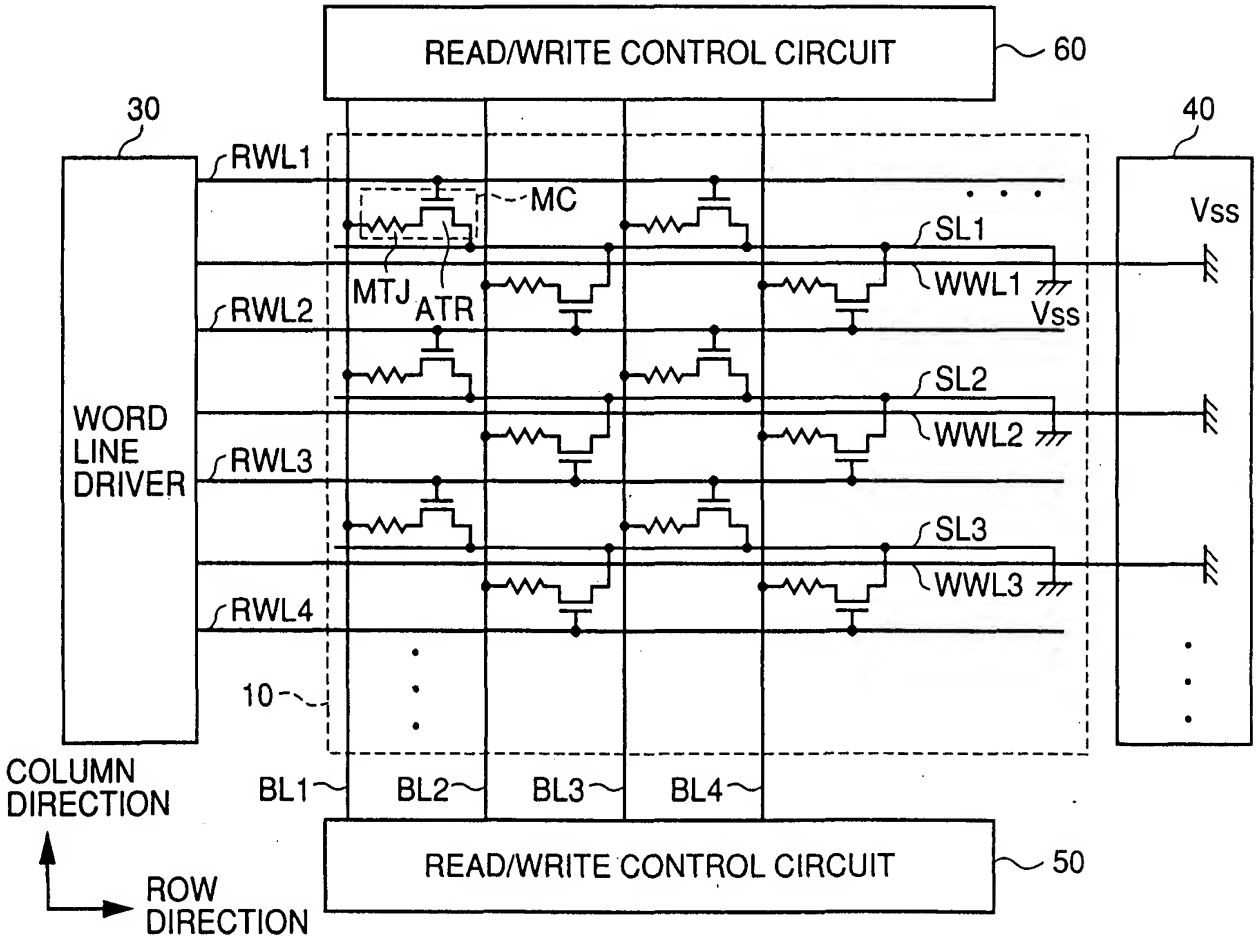
READ/WRITE CONTROL CIRCUIT
60
30
40
RWL1
MC
SL1
Vss
MTJ
ATR
WWL1
RWL2
Vss
SL2
WORD
LINE
DRIVER
WWL2
RWL3
SL3
WWL3
RWL4
10
COLUMN
DIRECTION
BL1
BL2
BL3
BL4
READ/WRITE CONTROL CIRCUIT
50
ROW
DIRECTION

FIG.37

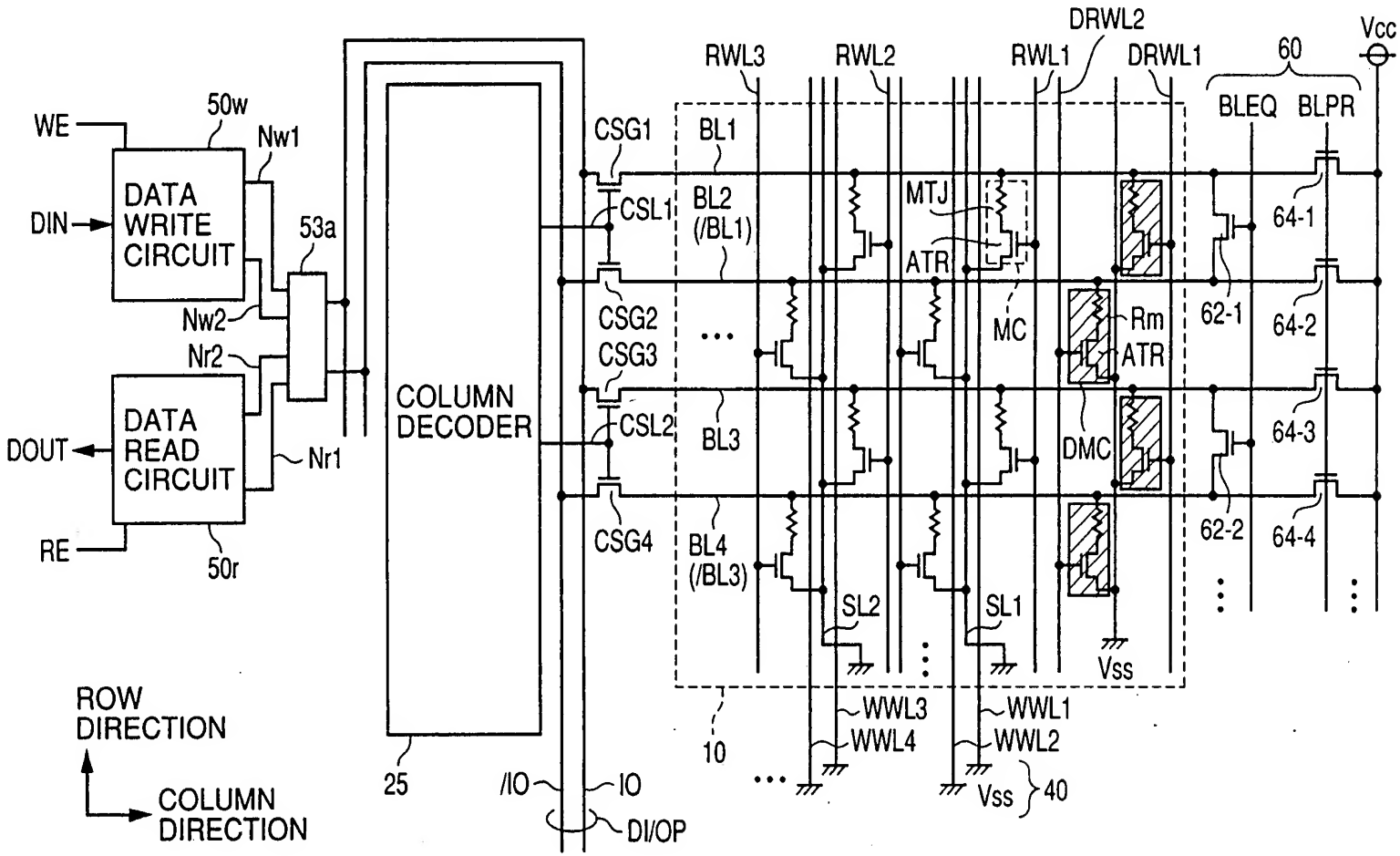
WE
50w
Nw1
DIN
DATA WRITE CIRCUIT
53a
Nw2
Nr2
DOUT
DATA READ CIRCUIT
Nr1
RE
50r
COLUMN DECODER
25
CSG1
CSL1
CSG2
CSG3
CSL2
CSG4
/IO
IO
DI/OP
RWL3
RWL2
RWL1
DRWL2
DRWL1
60
BLEQ
BLPR
Vcc
BL1
BL2 (/BL1)
BL3
BL4 (/BL3)
MTJ
ATR
MC
Rm
ATR
DMC
64-1
64-2
64-3
64-4
62-1
62-2
SL2
SL1
Vss
WWL3
WWL4
WWL1
WWL2
Vss
40
10
ROW DIRECTION
COLUMN DIRECTION

FIG.38

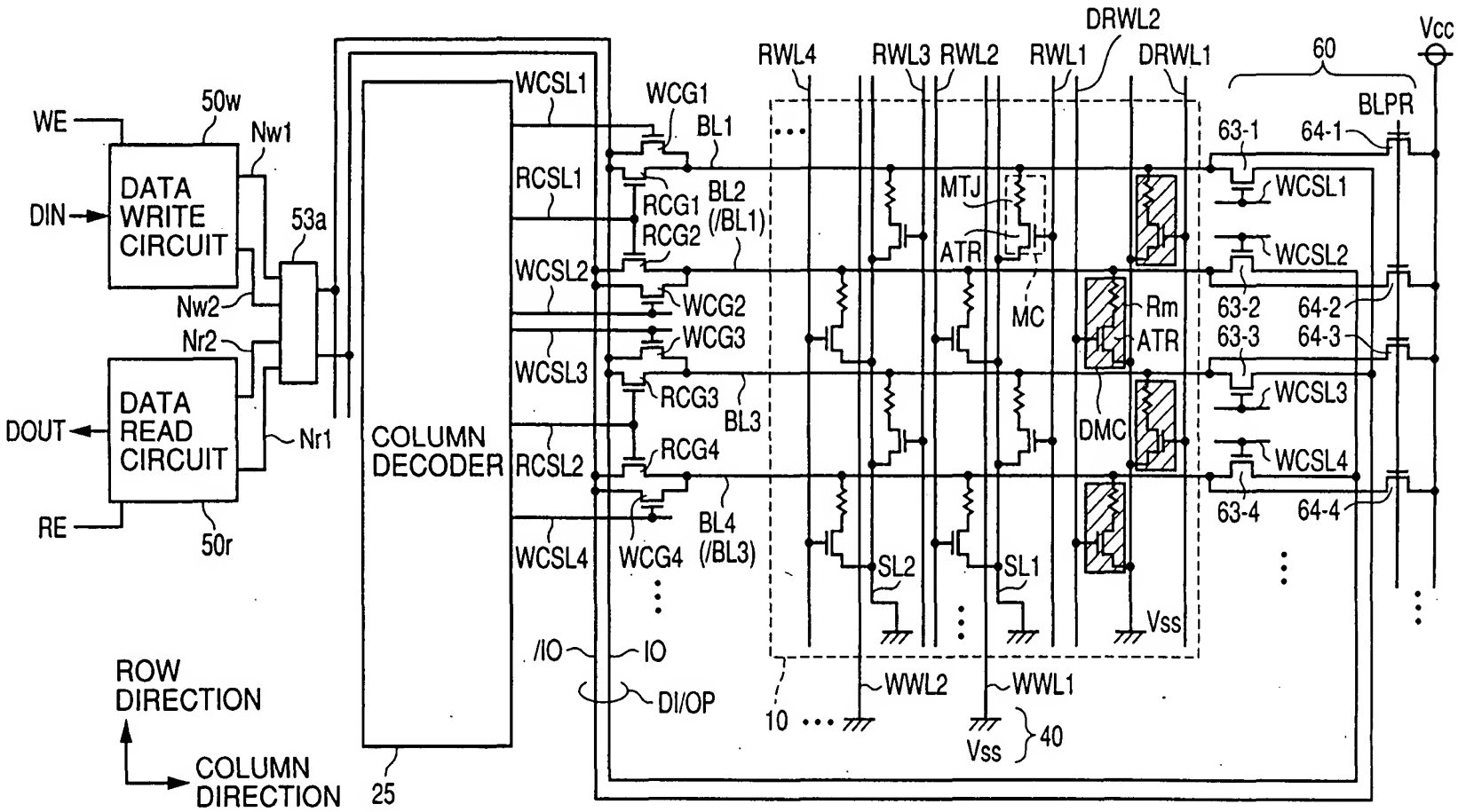
WE
50w
Nw1
DIN
DATA WRITE CIRCUIT
53a
Nw2
Nr2
DATA READ CIRCUIT
DOUT
Nr1
RE
50r
COLUMN DECODER
25
WCSL1
RCSL1
WCSL2
WCSL3
RCSL2
WCSL4
WCG1
BL1
RCG1
BL2 (/BL1)
RCG2
WCG2
WCG3
RCG3
BL3
RCG4
BL4 (/BL3)
WCG4
/IO
IO
DI/OP
ROW DIRECTION
COLUMN DIRECTION
RWL4
RWL3
RWL2
RWL1
DRWL2
DRWL1
60
Vcc
BLPR
63-1
64-1
MTJ
ATR
MC
Rm
ATR
DMC
63-2
64-2
63-3
64-3
63-4
64-4
WCSL1
WCSL2
WCSL3
WCSL4
SL2
SL1
Vss
WWL2
WWL1
10
Vss
40

FIG.39

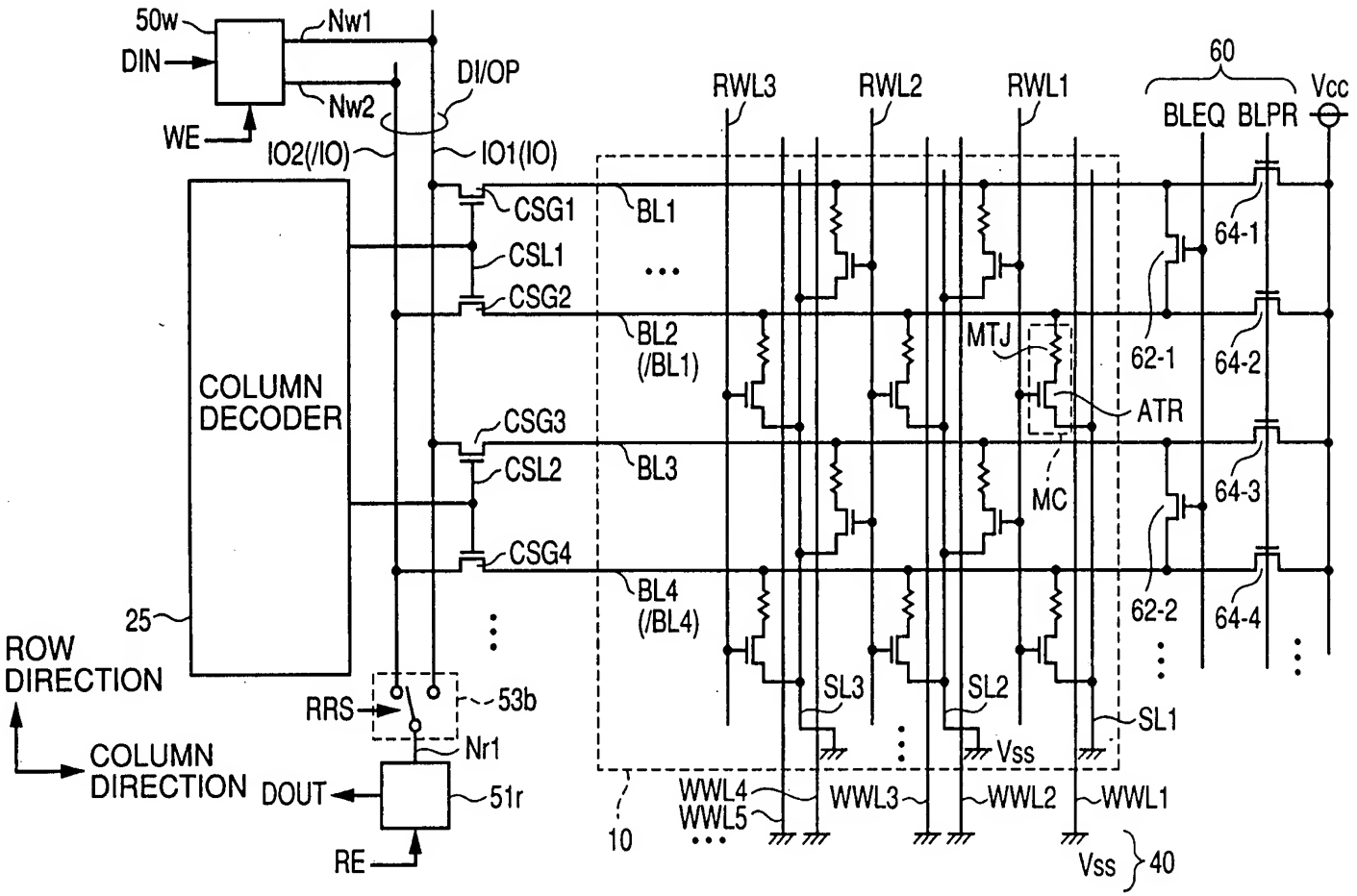
50w
DIN
WE
Nw1
Nw2
DI/OP
IO2(/IO)
IO1(IO)
COLUMN DECODER
25
CSG1
CSL1
CSG2
CSG3
CSL2
CSG4
BL1
BL2 (/BL1)
BL3
BL4 (/BL4)
RWL3
RWL2
RWL1
60
BLEQ
BLPR
Vcc
64-1
64-2
64-3
64-4
62-1
62-2
MTJ
ATR
MC
SL3
SL2
SL1
Vss
WWL4
WWL5
WWL3
WWL2
WWL1
40
10
ROW DIRECTION
COLUMN DIRECTION
RRS
53b
Nr1
DOUT
51r
RE

FIG.40

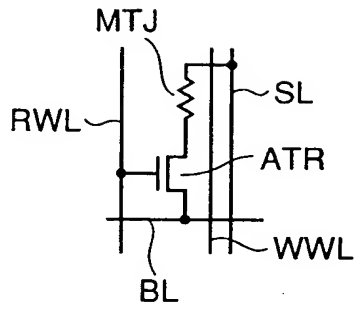
MTJ
SL
RWL
ATR
WWL
BL

FIG.41

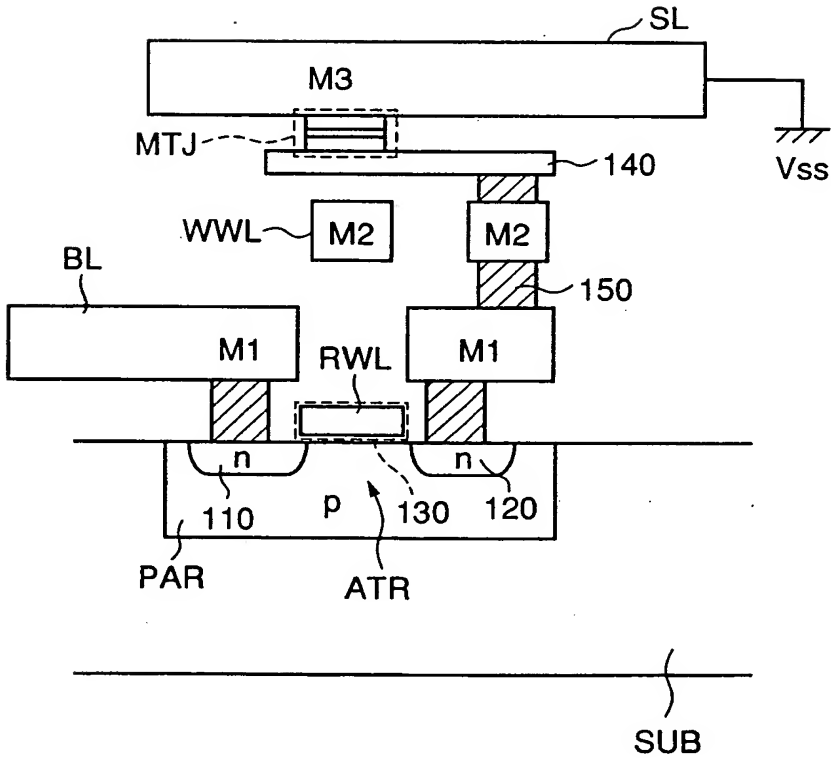
SL
M3
MTJ
140
Vss
WWL
M2
M2
BL
150
M1
RWL
M1
n
n
110
P
130
120
PAR
ATR
SUB

FIG.42

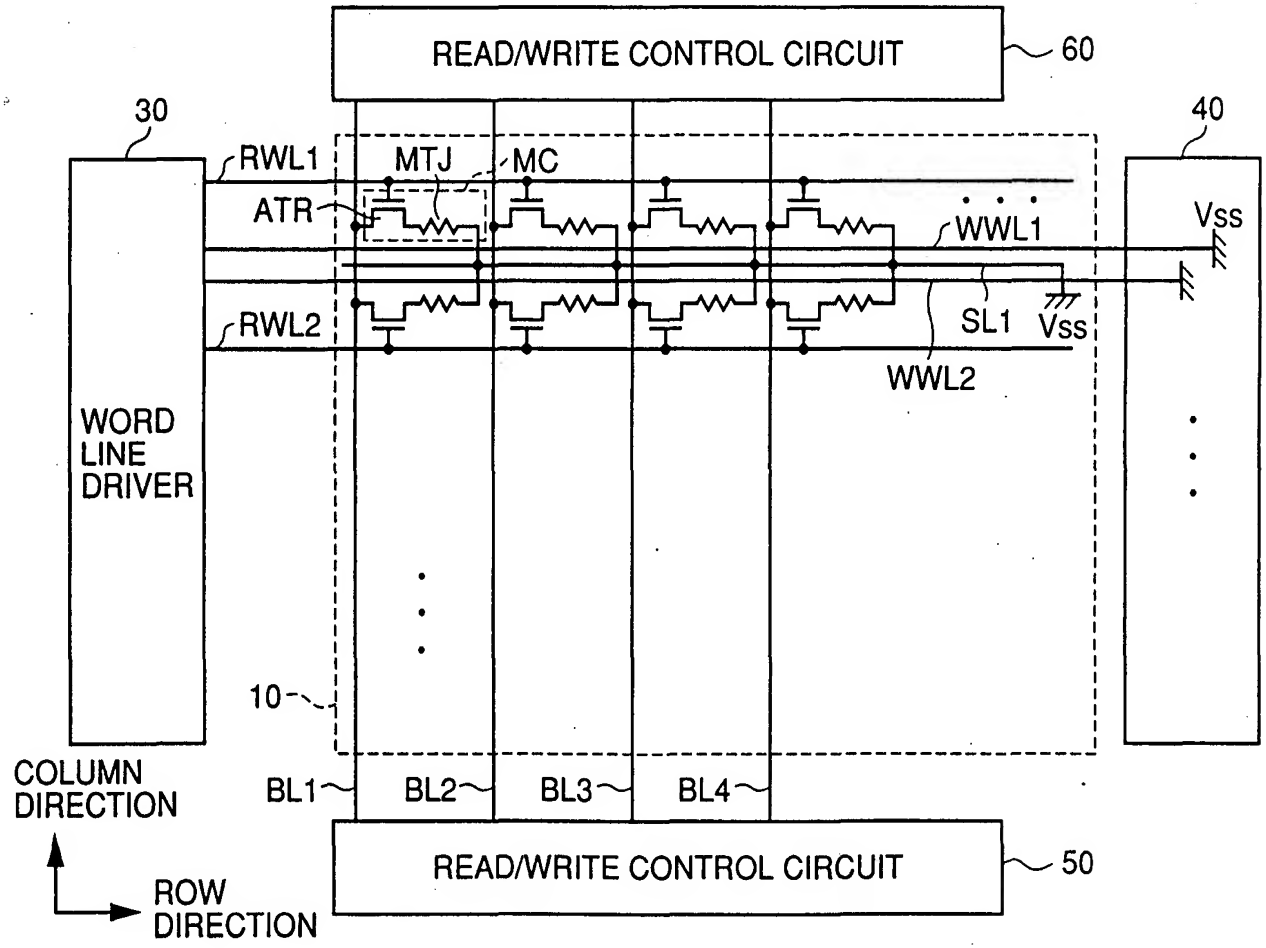
READ/WRITE CONTROL CIRCUIT
60
30
40
RWL1
MTJ
MC
ATR
WWL1
Vss
RWL2
SL1
Vss
WWL2
WORD
LINE
DRIVER
10
COLUMN
DIRECTION
BL1
BL2
BL3
BL4
READ/WRITE CONTROL CIRCUIT
50
ROW
DIRECTION

FIG.43

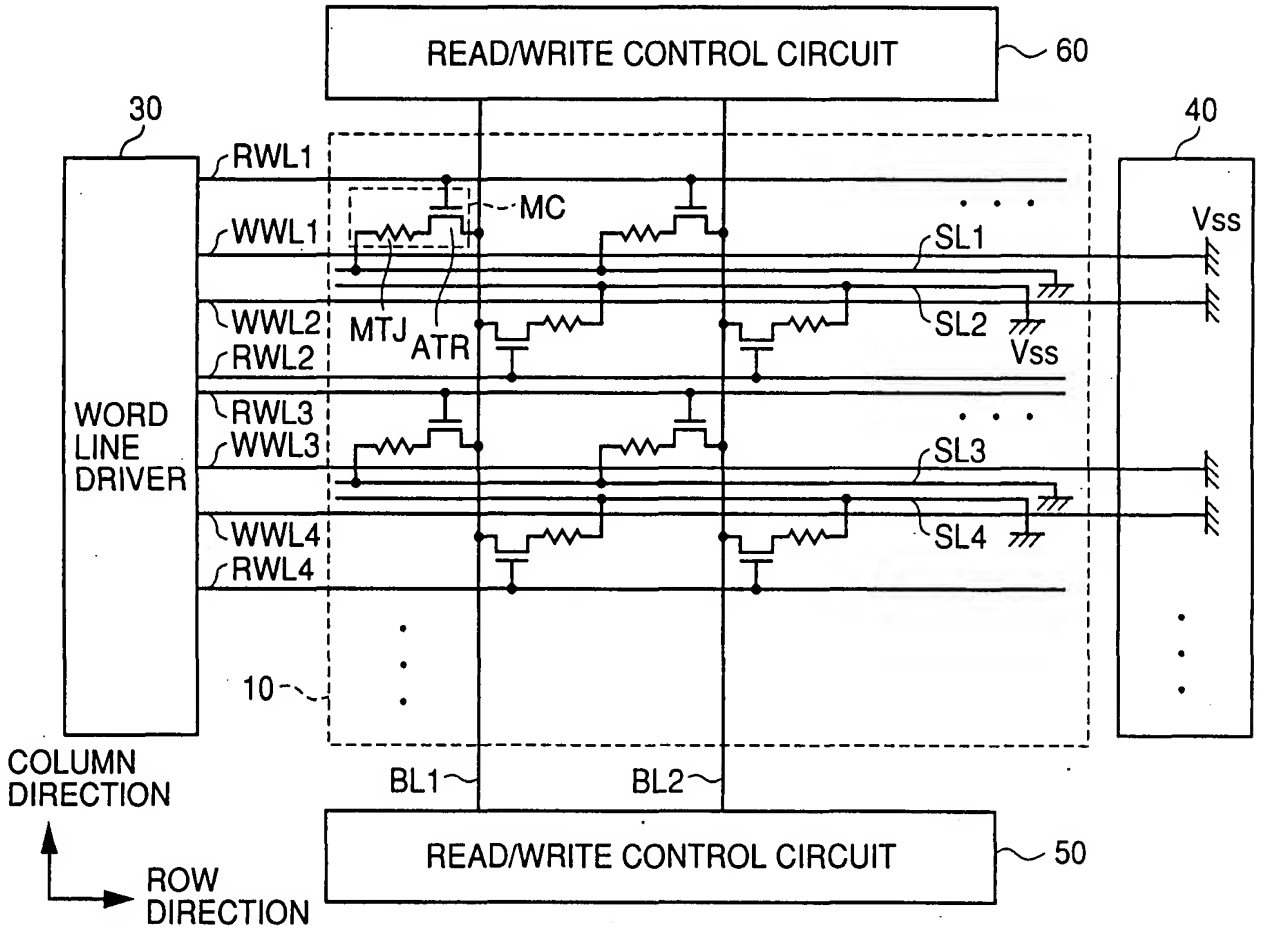
READ/WRITE CONTROL CIRCUIT
60
30
40
RWL1
WWL1
MC
SL1
Vss
WWL2
MTJ
ATR
SL2
Vss
RWL2
RWL3
WORD
LINE
DRIVER
WWL3
SL3
WWL4
SL4
RWL4
10
BL1
BL2
COLUMN
DIRECTION
ROW
DIRECTION
READ/WRITE CONTROL CIRCUIT
50

FIG.44

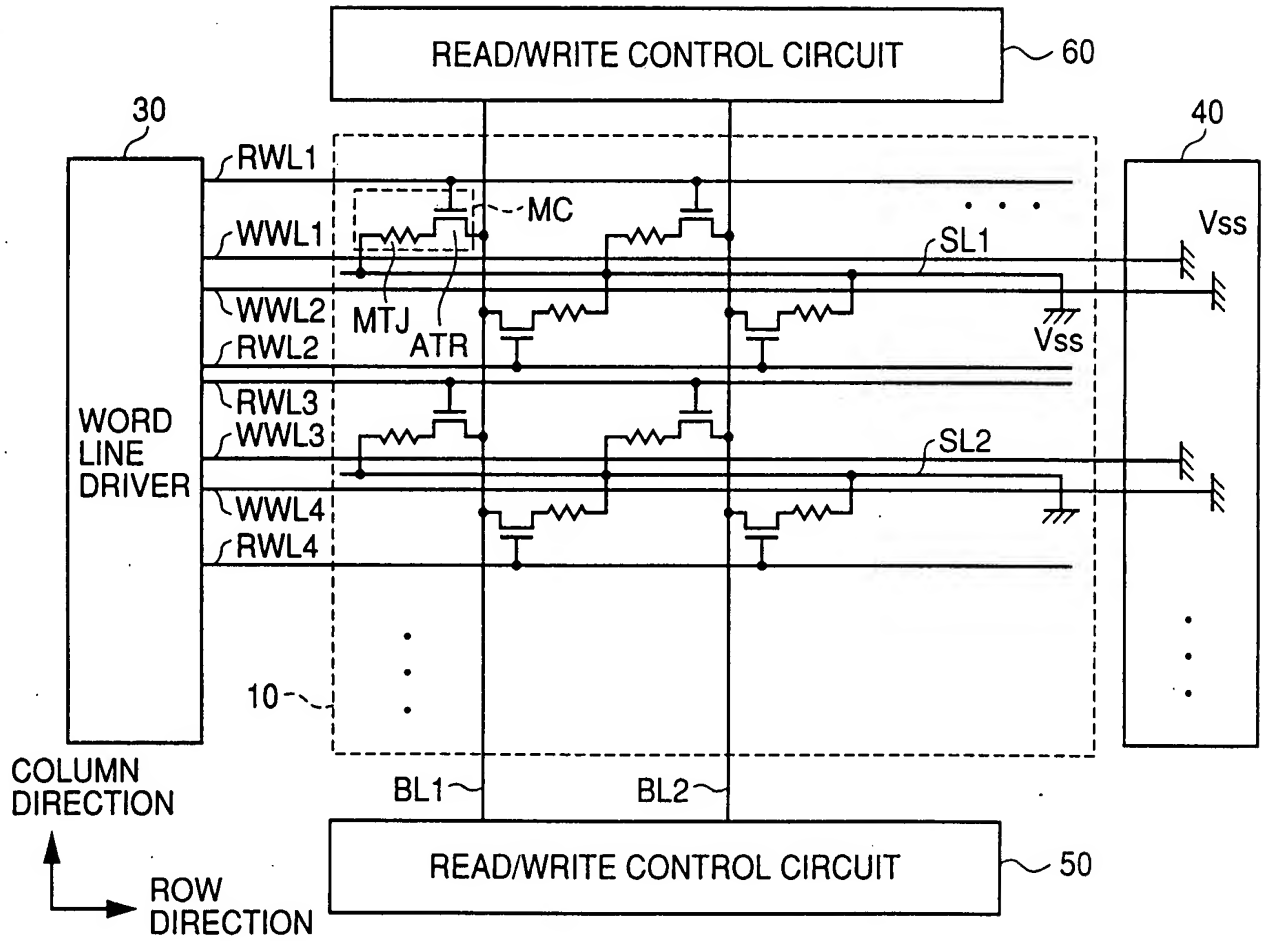
READ/WRITE CONTROL CIRCUIT
60
30
40
RWL1
WWL1
WWL2
RWL2
RWL3
WWL3
WWL4
RWL4
WORD LINE DRIVER
MC
MTJ
ATR
SL1
SL2
Vss
Vss
10
BL1
BL2
COLUMN DIRECTION
ROW DIRECTION
READ/WRITE CONTROL CIRCUIT
50

FIG.45

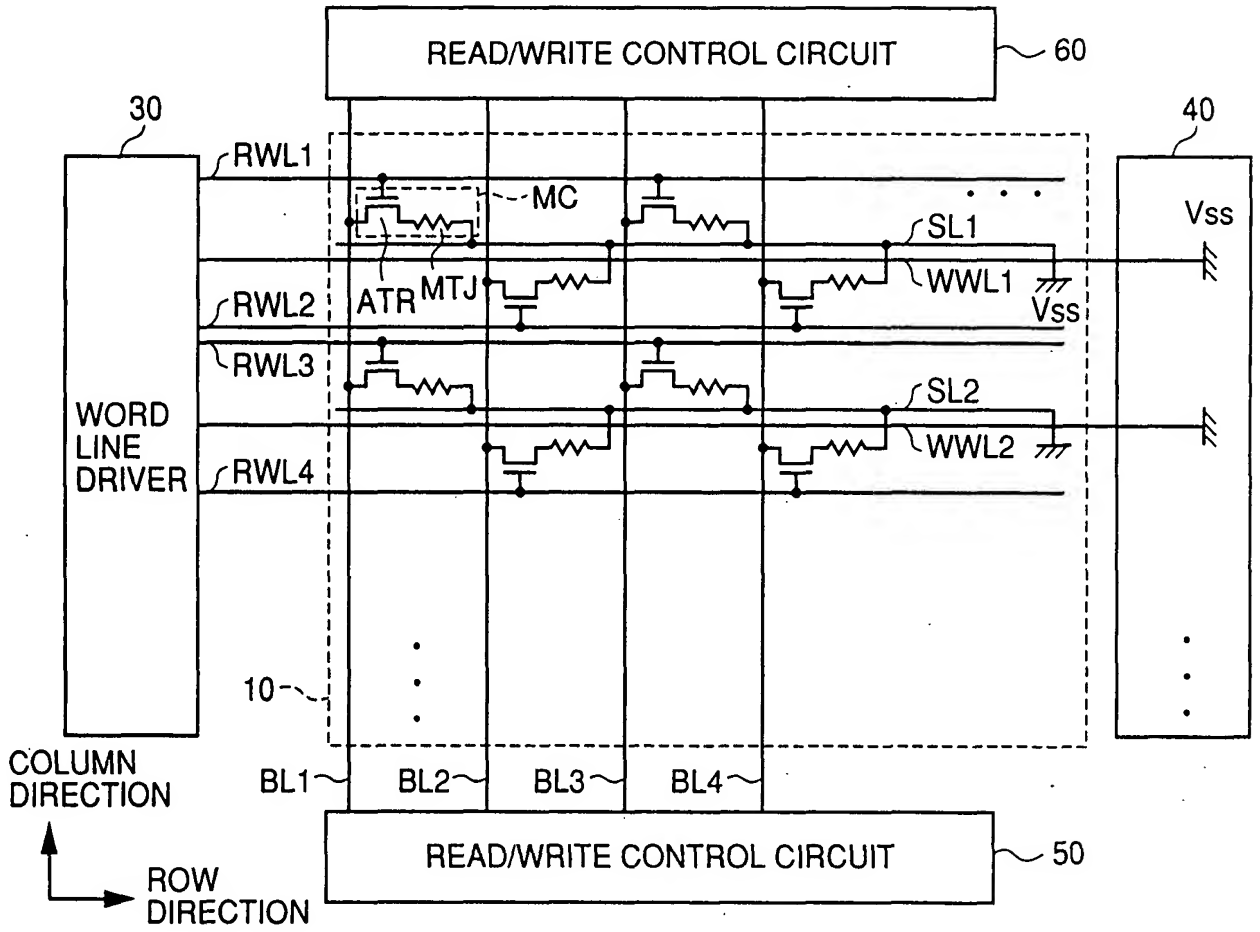
READ/WRITE CONTROL CIRCUIT
60
30
40
RWL1
MC
SL1
Vss
ATR
MTJ
WWL1
RWL2
Vss
RWL3
SL2
WORD
LINE
DRIVER
WWL2
RWL4
10
COLUMN
DIRECTION
BL1
BL2
BL3
BL4
READ/WRITE CONTROL CIRCUIT
50
ROW
DIRECTION

FIG.46

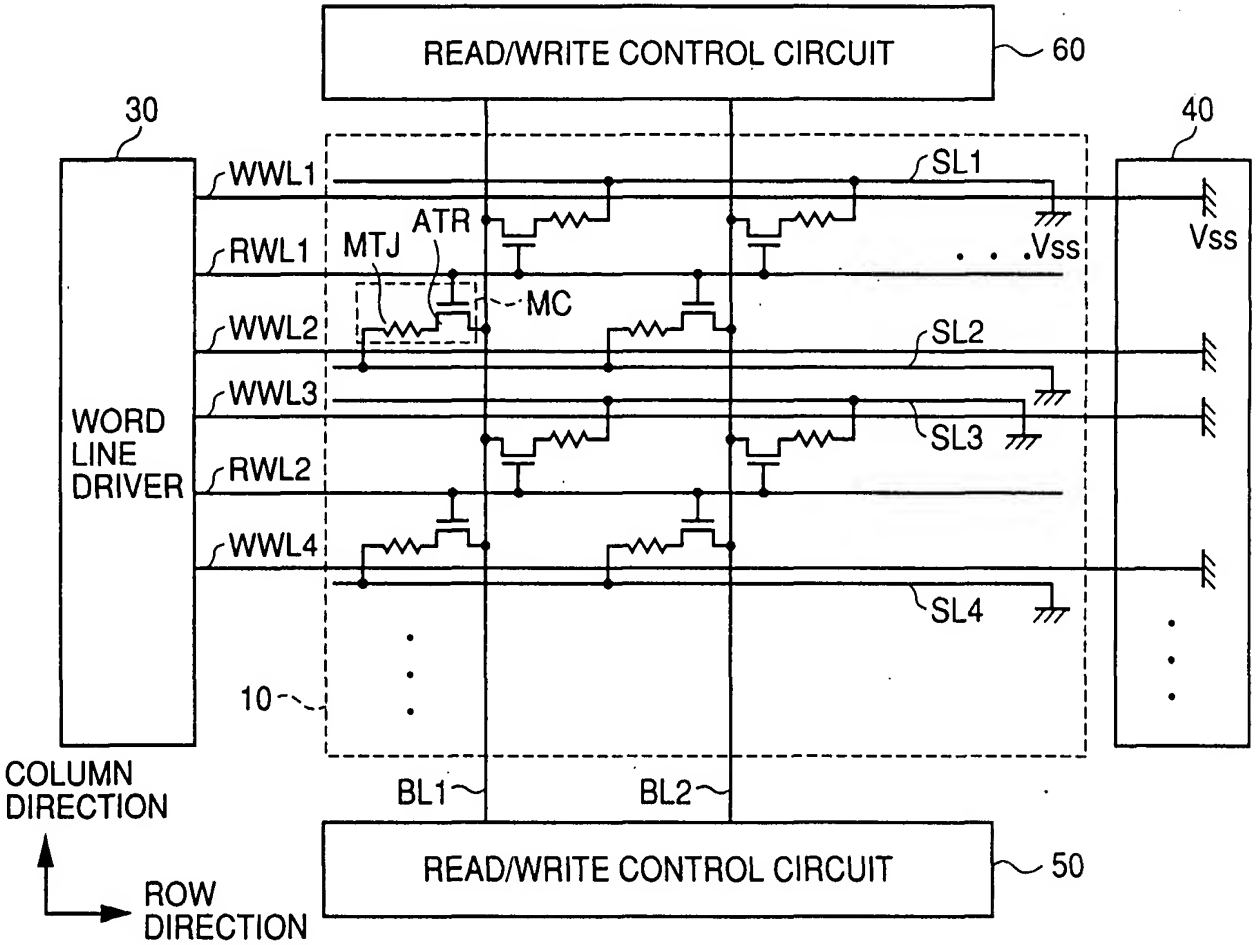
READ/WRITE CONTROL CIRCUIT
60
30
40
WWL1
SL1
ATR
RWL1
MTJ
Vss
Vss
MC
WWL2
SL2
WWL3
SL3
WORD LINE DRIVER
RWL2
WWL4
SL4
10
BL1
BL2
COLUMN DIRECTION
ROW DIRECTION
READ/WRITE CONTROL CIRCUIT
50

FIG.47

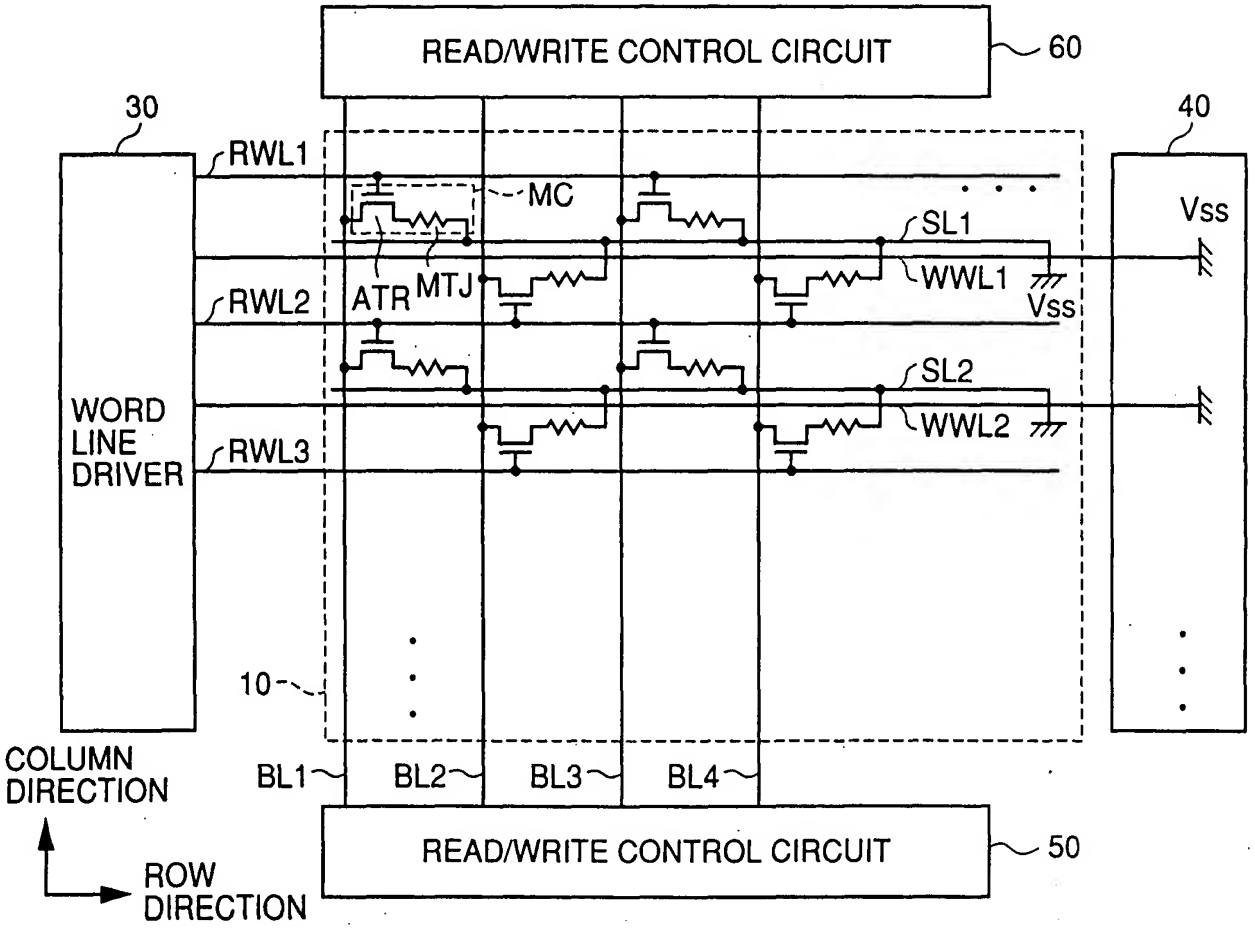
READ/WRITE CONTROL CIRCUIT
60
30
40
RWL1
MC
SL1
Vss
ATR
MTJ
RWL2
WWL1
Vss
SL2
WORD
LINE
DRIVER
RWL3
WWL2
10
COLUMN
DIRECTION
BL1
BL2
BL3
BL4
READ/WRITE CONTROL CIRCUIT
50
ROW
DIRECTION

FIG.48

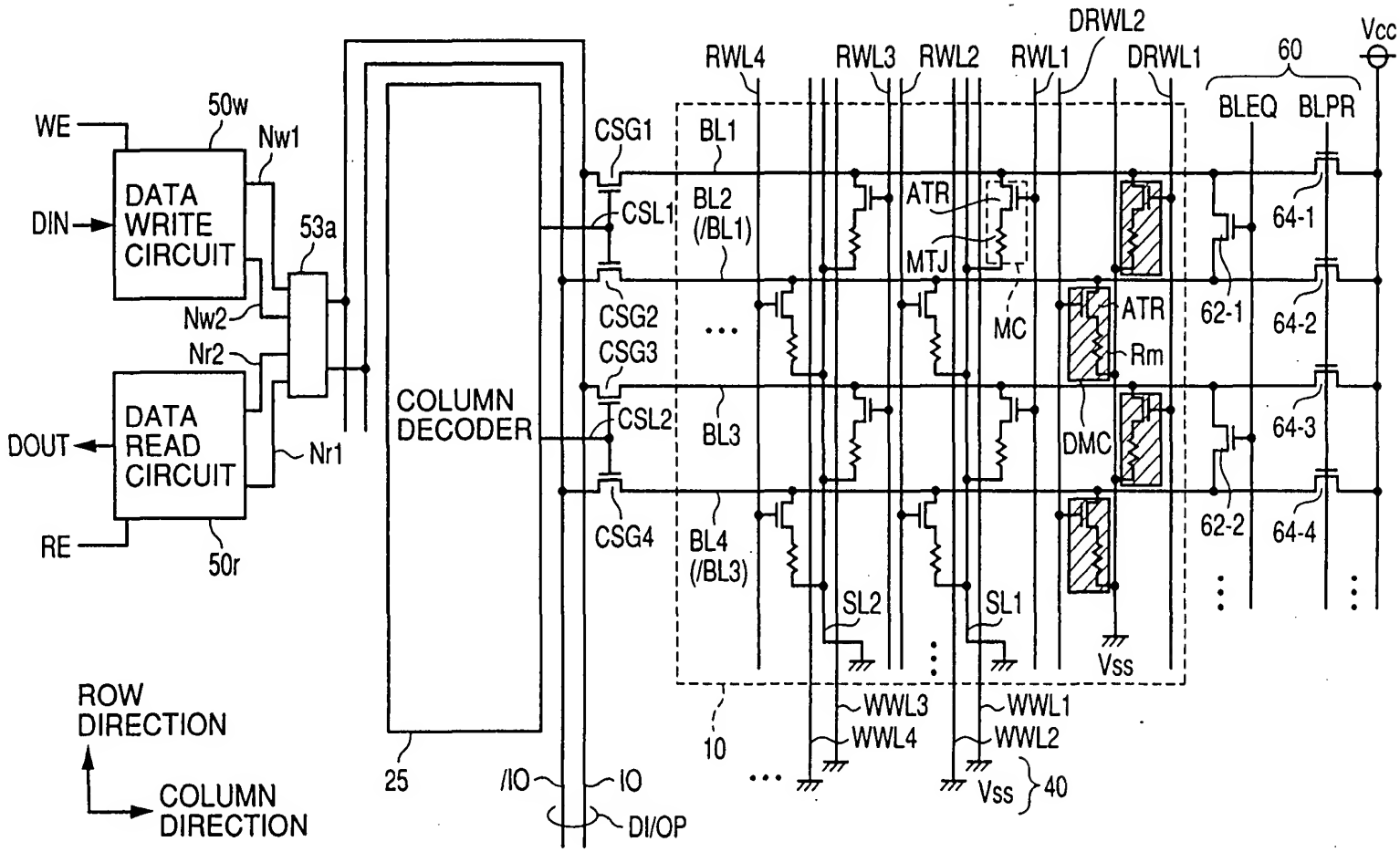
WE
50w
Nw1
DIN
DATA WRITE CIRCUIT
53a
Nw2
Nr2
DATA READ CIRCUIT
DOUT
Nr1
RE
50r
COLUMN DECODER
25
CSG1
CSL1
CSG2
CSG3
CSL2
CSG4
/IO
IO
DI/OP
RWL4
RWL3
RWL2
RWL1
DRWL2
DRWL1
60
BLEQ
BLPR
Vcc
BL1
BL2 (/BL1)
BL3
BL4 (/BL3)
ATR
MTJ
MC
DMC
Rm
64-1
64-2
64-3
64-4
62-1
62-2
SL2
SL1
Vss
WWL3
WWL4
WWL1
WWL2
10
40
ROW DIRECTION
COLUMN DIRECTION

FIG.49

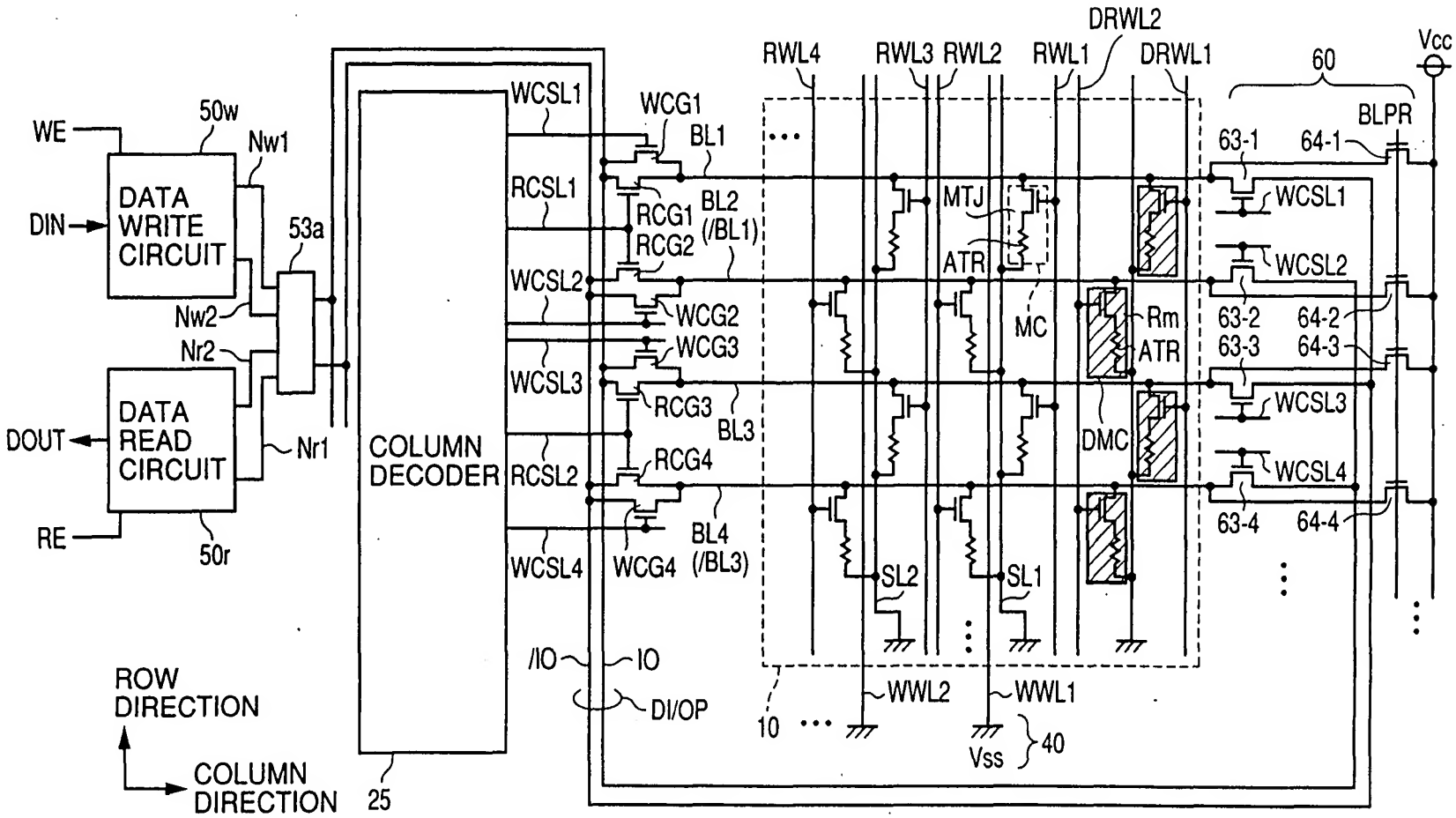
WE
DIN
DOUT
RE
50w
Nw1
Nw2
Nr2
Nr1
50r
DATA WRITE CIRCUIT
DATA READ CIRCUIT
53a
COLUMN DECODER
25
WCSL1
RCSL1
WCSL2
WCSL3
RCSL2
WCSL4
WCG1
RCG1
WCG2
RCG2
WCG3
RCG3
WCG4
RCG4
BL1
BL2 (/BL1)
BL3
BL4 (/BL3)
/IO
IO
DI/OP
ROW DIRECTION
COLUMN DIRECTION
RWL4
RWL3
RWL2
RWL1
DRWL2
DRWL1
MTJ
ATR
MC
DMC
Rm
ATR
SL2
SL1
WWL2
WWL1
10
Vss
40
60
BLPR
63-1
64-1
63-2
64-2
63-3
64-3
63-4
64-4
WCSL1
WCSL2
WCSL3
WCSL4
Vcc

FIG.50

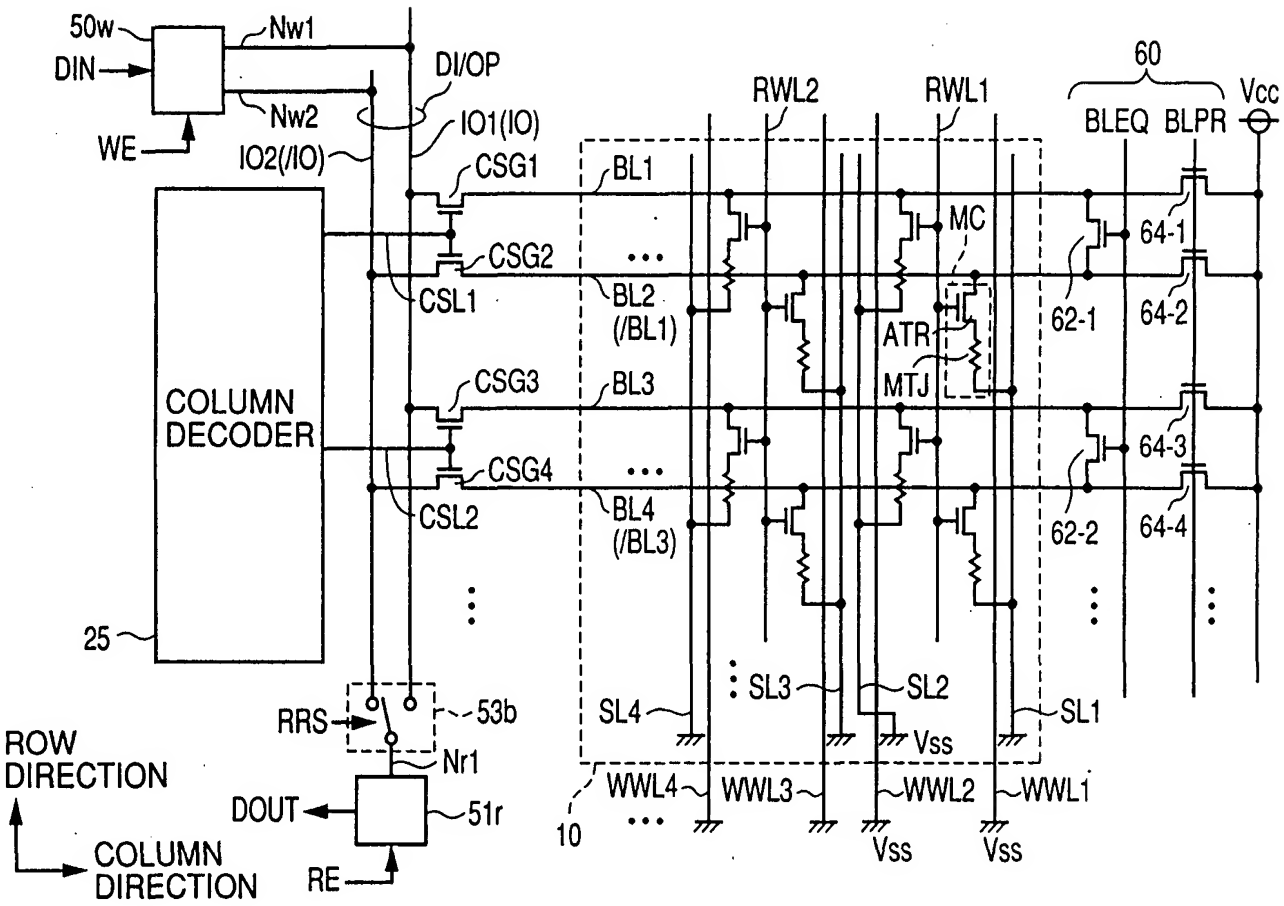
50w
DIN
WE
Nw1
Nw2
DI/OP
IO1(IO)
IO2(/IO)
CSG1
CSG2
CSG3
CSG4
CSL1
CSL2
COLUMN DECODER
25
BL1
BL2 (/BL1)
BL3
BL4 (/BL3)
RWL2
RWL1
MC
ATR
MTJ
60
BLEQ
BLPR
Vcc
64-1
64-2
64-3
64-4
62-1
62-2
SL4
SL3
SL2
SL1
Vss
WWL4
WWL3
WWL2
WWL1
10
RRS
53b
Nr1
DOUT
51r
RE
ROW DIRECTION
COLUMN DIRECTION

FIG.51

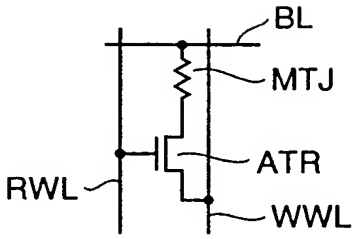
BL
MTJ
ATR
RWL
WWL

FIG.52

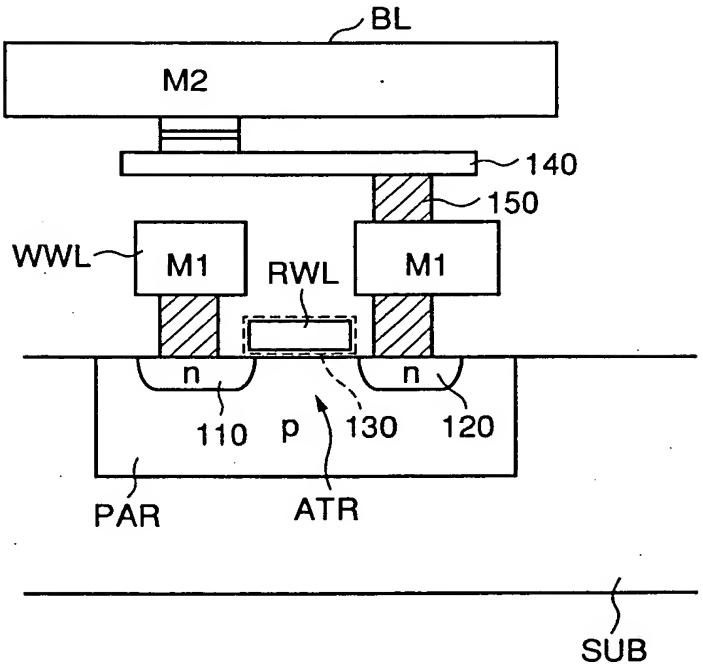
BL
M2
140
150
WWL
M1
RWL
M1
n
n
110
p
130
120
PAR
ATR
SUB

FIG.53

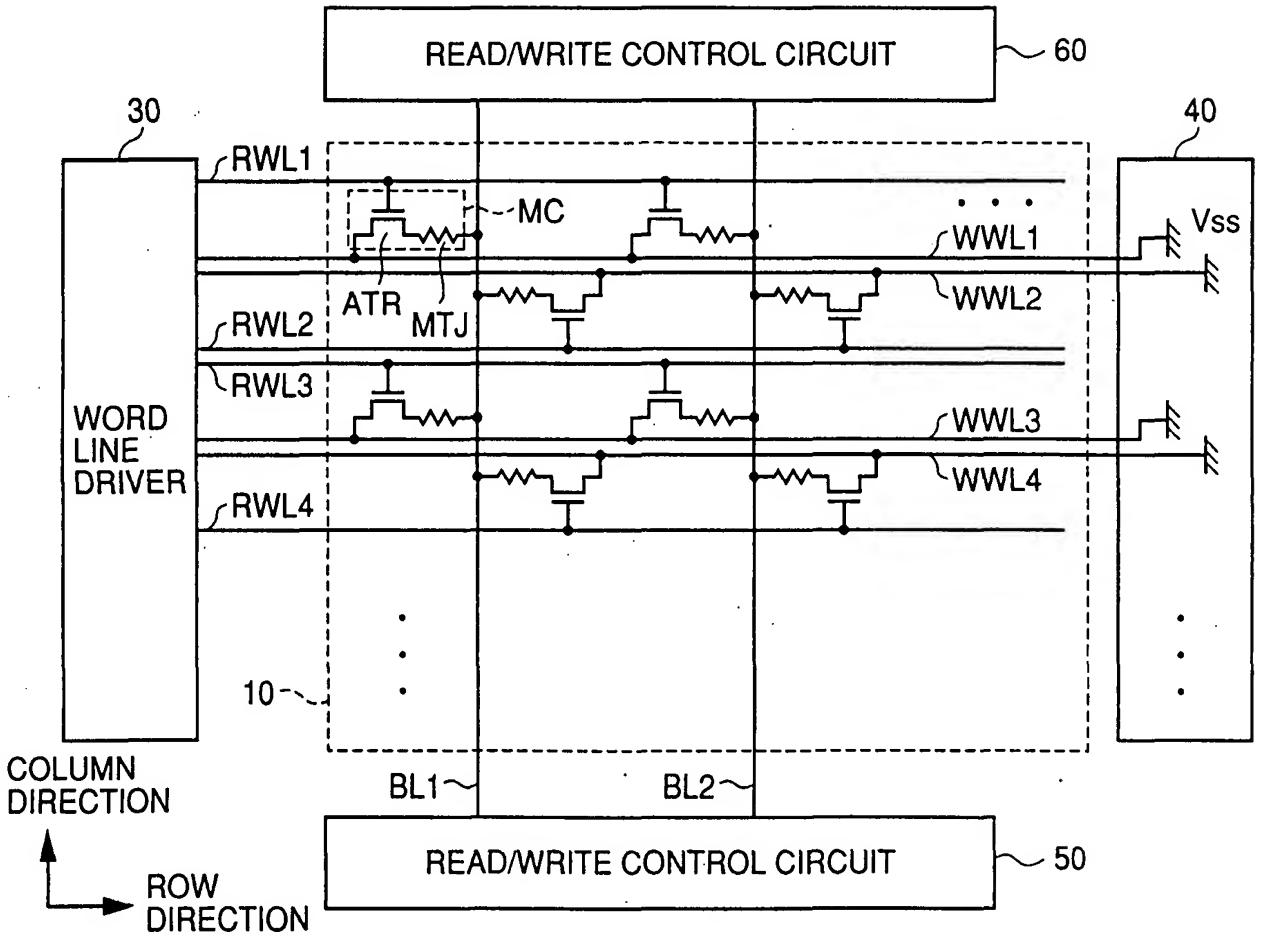
READ/WRITE CONTROL CIRCUIT
60
30
40
RWL1
MC
WWL1
Vss
ATR
MTJ
WWL2
RWL2
RWL3
WORD
LINE
DRIVER
WWL3
WWL4
RWL4
10
COLUMN
DIRECTION
BL1
BL2
READ/WRITE CONTROL CIRCUIT
50
ROW
DIRECTION

FIG.54

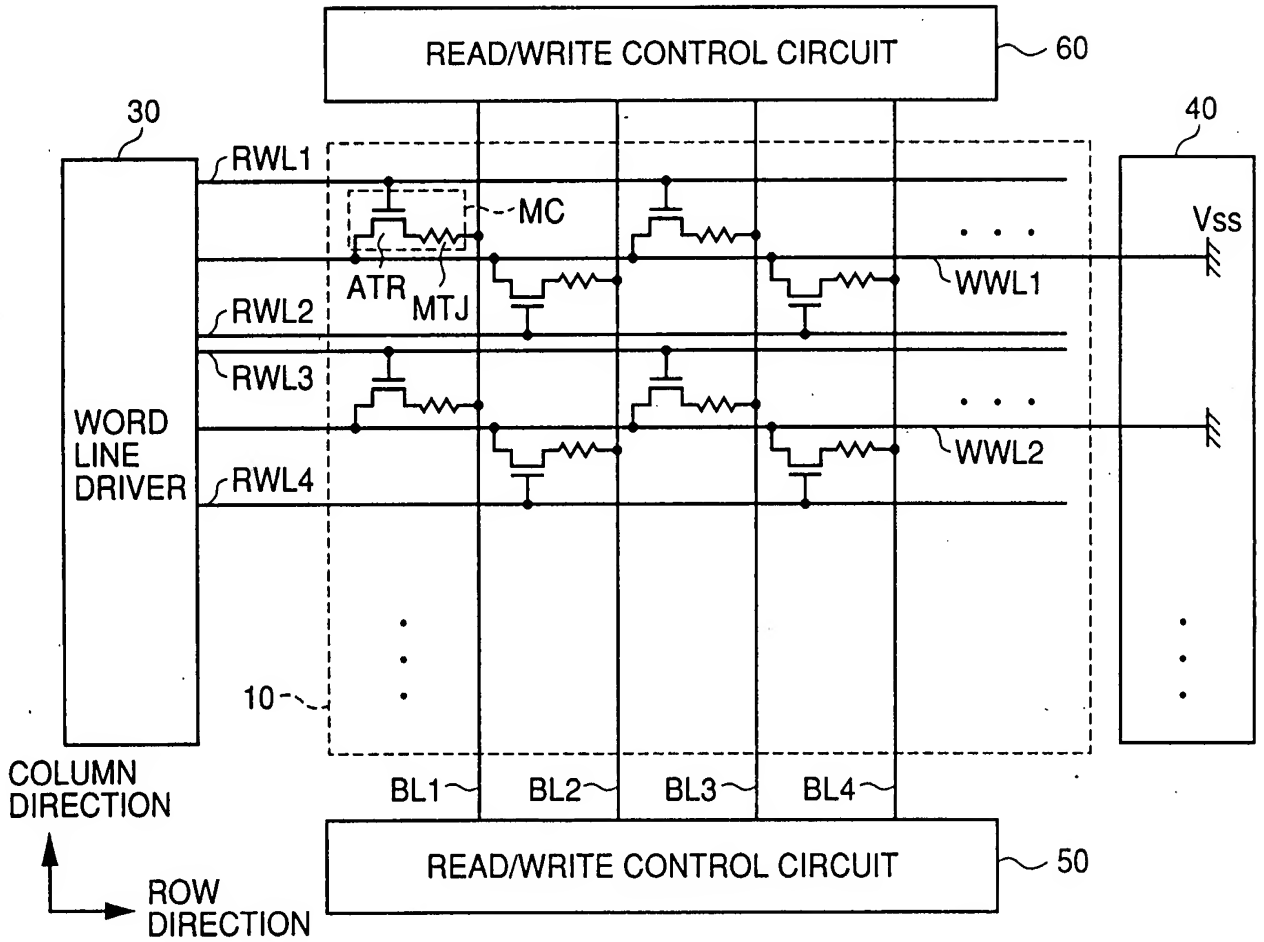
READ/WRITE CONTROL CIRCUIT
60
30
40
RWL1
MC
Vss
ATR
MTJ
WWL1
RWL2
RWL3
WORD LINE DRIVER
WWL2
RWL4
10
BL1
BL2
BL3
BL4
COLUMN DIRECTION
ROW DIRECTION
READ/WRITE CONTROL CIRCUIT
50

FIG.55

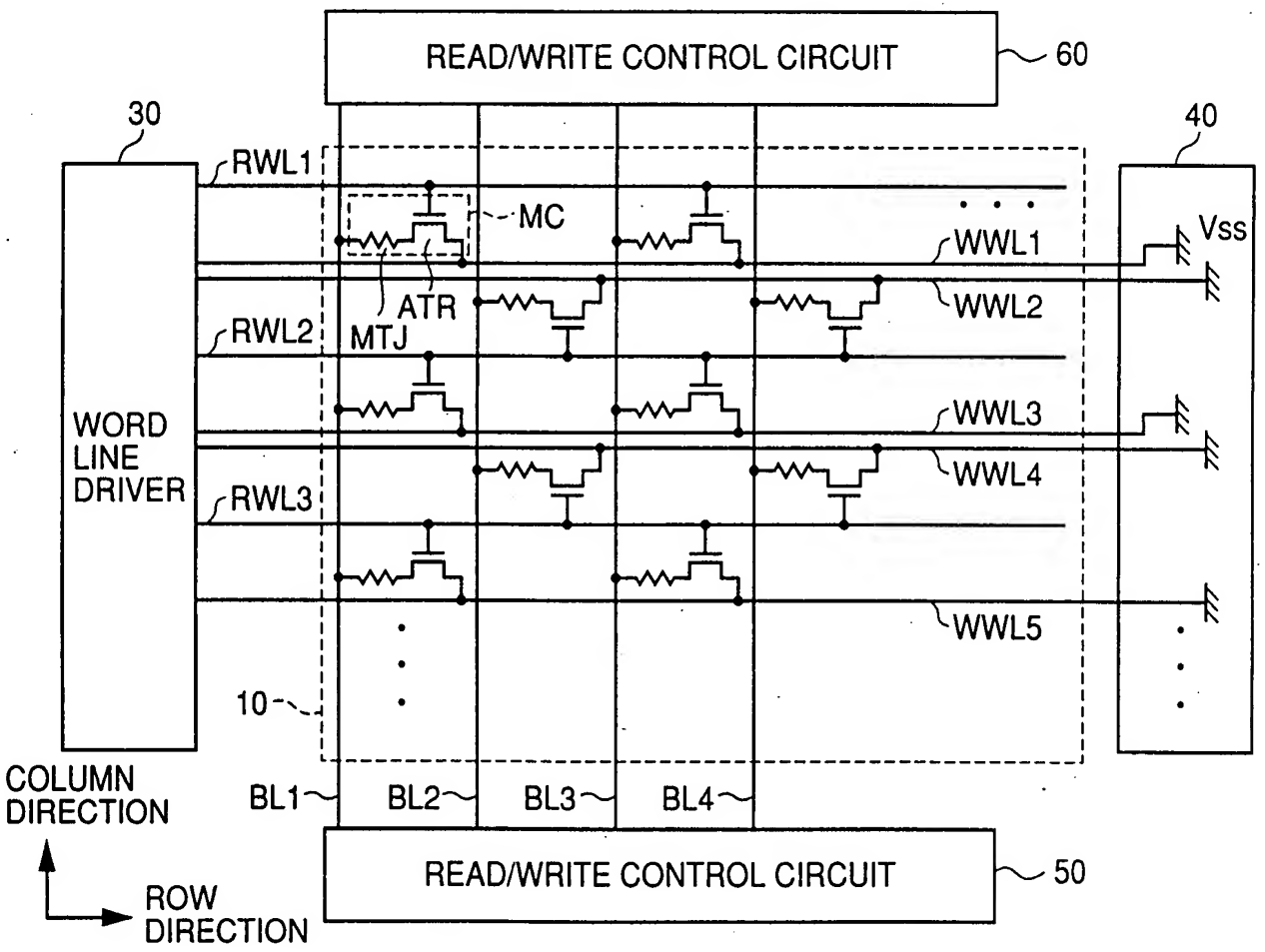
READ/WRITE CONTROL CIRCUIT
60
30
40
RWL1
MC
WWL1
Vss
ATR
MTJ
RWL2
WWL2
WORD
LINE
DRIVER
WWL3
RWL3
WWL4
WWL5
10
COLUMN
DIRECTION
BL1
BL2
BL3
BL4
READ/WRITE CONTROL CIRCUIT
50
ROW
DIRECTION

FIG.56

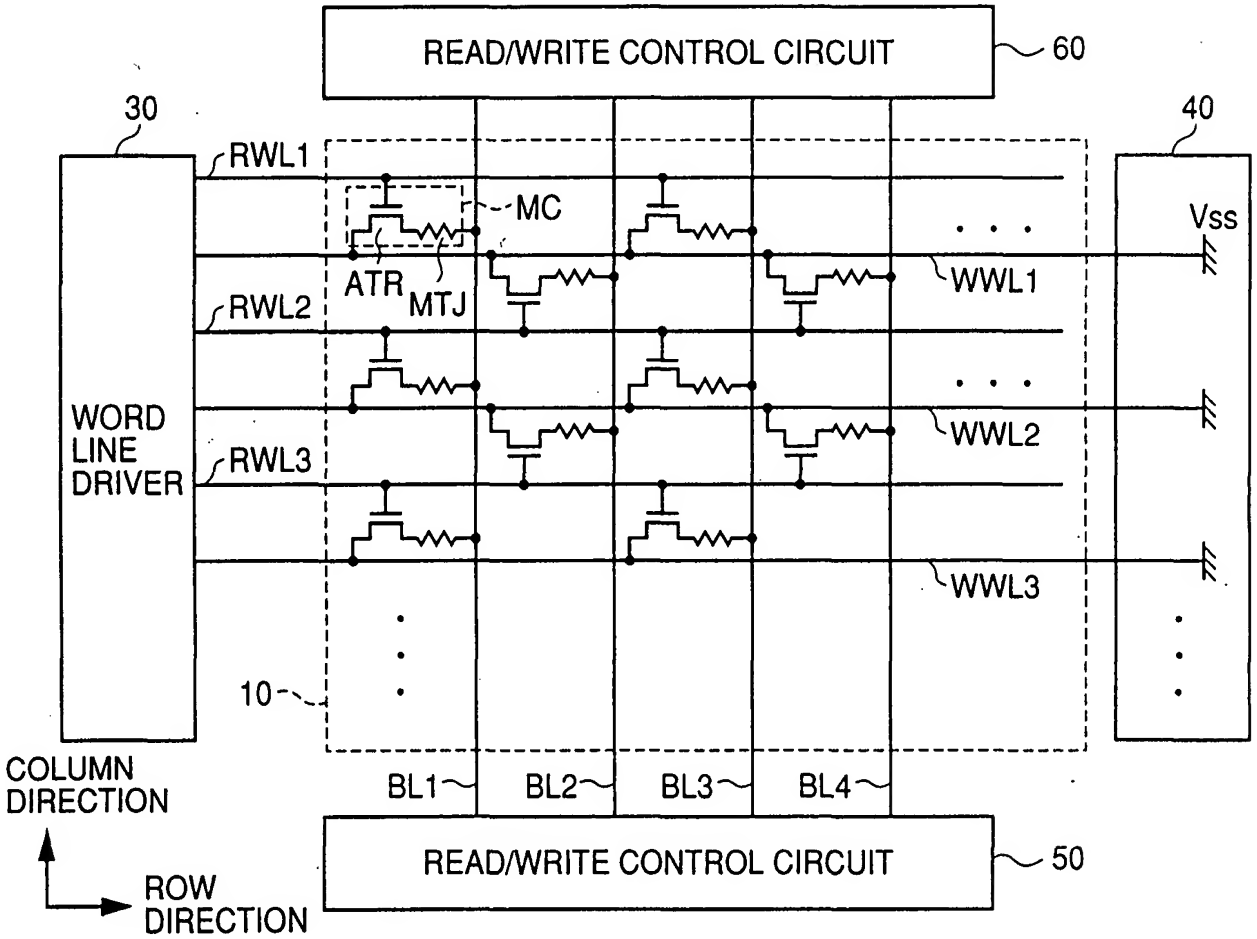
READ/WRITE CONTROL CIRCUIT
60
30
40
RWL1
MC
Vss
ATR
MTJ
WWL1
RWL2
WORD
LINE
DRIVER
WWL2
RWL3
WWL3
10
BL1
BL2
BL3
BL4
COLUMN
DIRECTION
ROW
DIRECTION
READ/WRITE CONTROL CIRCUIT
50

FIG.57

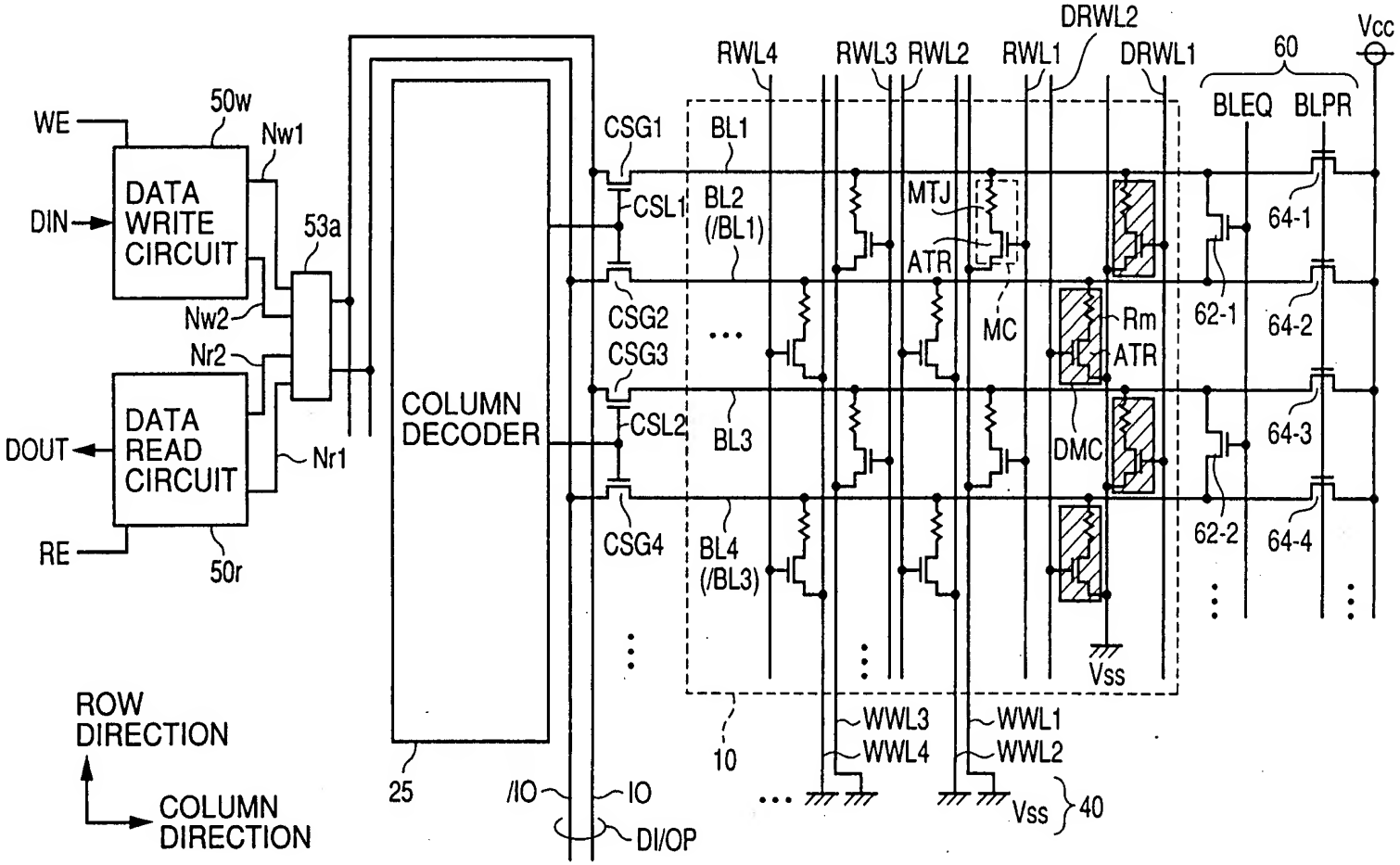
WE
50w
Nw1
DIN
DATA WRITE CIRCUIT
53a
Nw2
Nr2
DOUT
DATA READ CIRCUIT
Nr1
RE
50r
COLUMN DECODER
25
CSG1
CSL1
CSG2
CSG3
CSL2
CSG4
BL1
BL2 (/BL1)
BL3
BL4 (/BL3)
RWL4
RWL3
RWL2
RWL1
DRWL2
DRWL1
60
BLEQ
BLPR
Vcc
MTJ
ATR
MC
Rm
ATR
DMC
64-1
64-2
64-3
64-4
62-1
62-2
Vss
10
WWL3
WWL4
WWL1
WWL2
Vss
40
/IO
IO
DI/OP
ROW DIRECTION
COLUMN DIRECTION

FIG.58

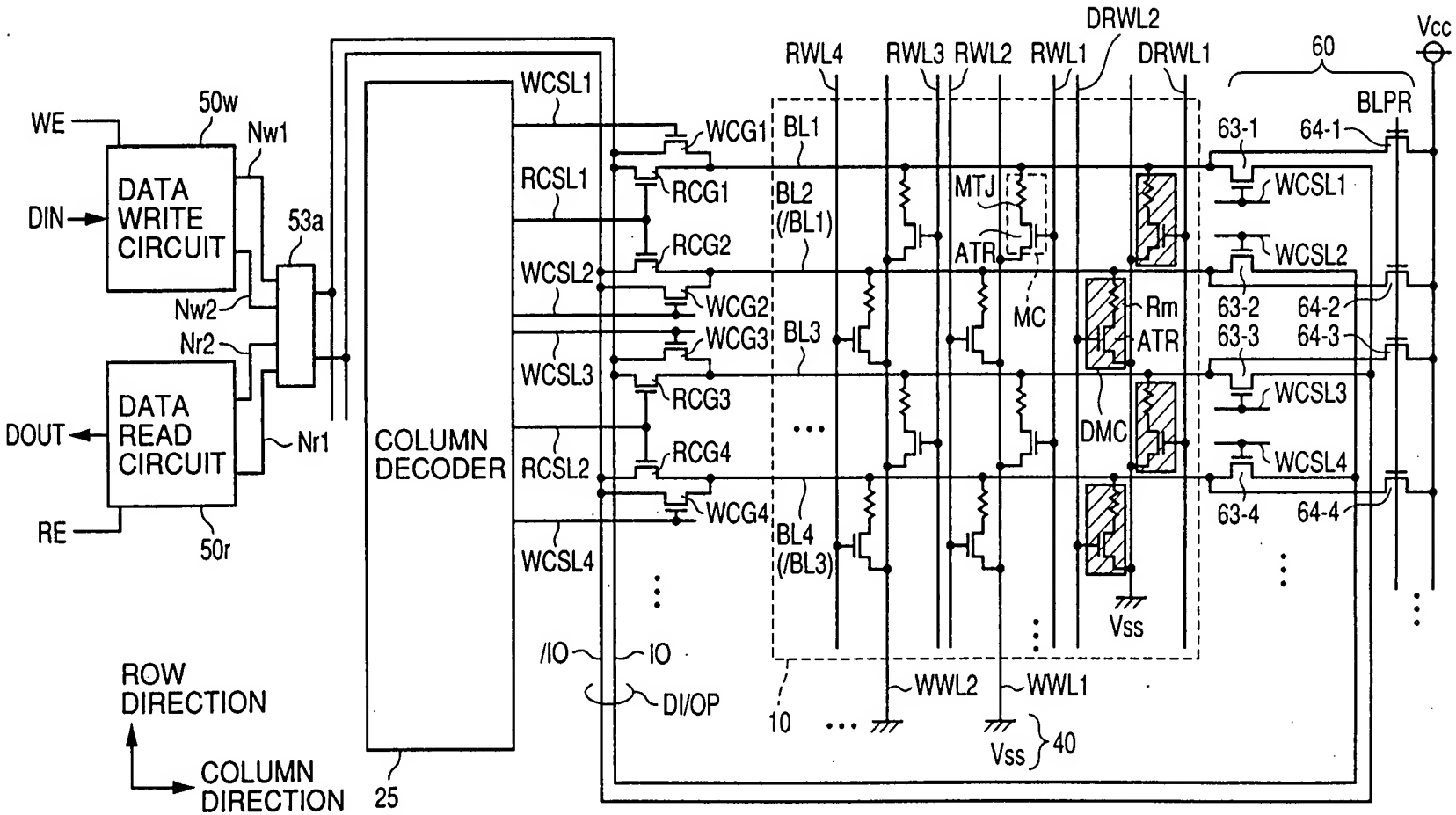
WE
50w
Nw1
DIN
DATA WRITE CIRCUIT
53a
Nw2
Nr2
DATA READ CIRCUIT
DOUT
Nr1
RE
50r
COLUMN DECODER
25
WCSL1
RCSL1
WCSL2
WCSL3
RCSL2
WCSL4
WCG1
RCG1
RCG2
WCG2
WCG3
RCG3
RCG4
WCG4
/IO
IO
DI/OP
ROW DIRECTION
COLUMN DIRECTION
RWL4
RWL3
RWL2
RWL1
DRWL2
DRWL1
BL1
BL2 (/BL1)
BL3
BL4 (/BL3)
MTJ
ATR
MC
Rm
DMC
Vss
10
WWL2
WWL1
40
60
Vcc
BLPR
63-1
64-1
63-2
64-2
63-3
64-3
63-4
64-4

FIG.59

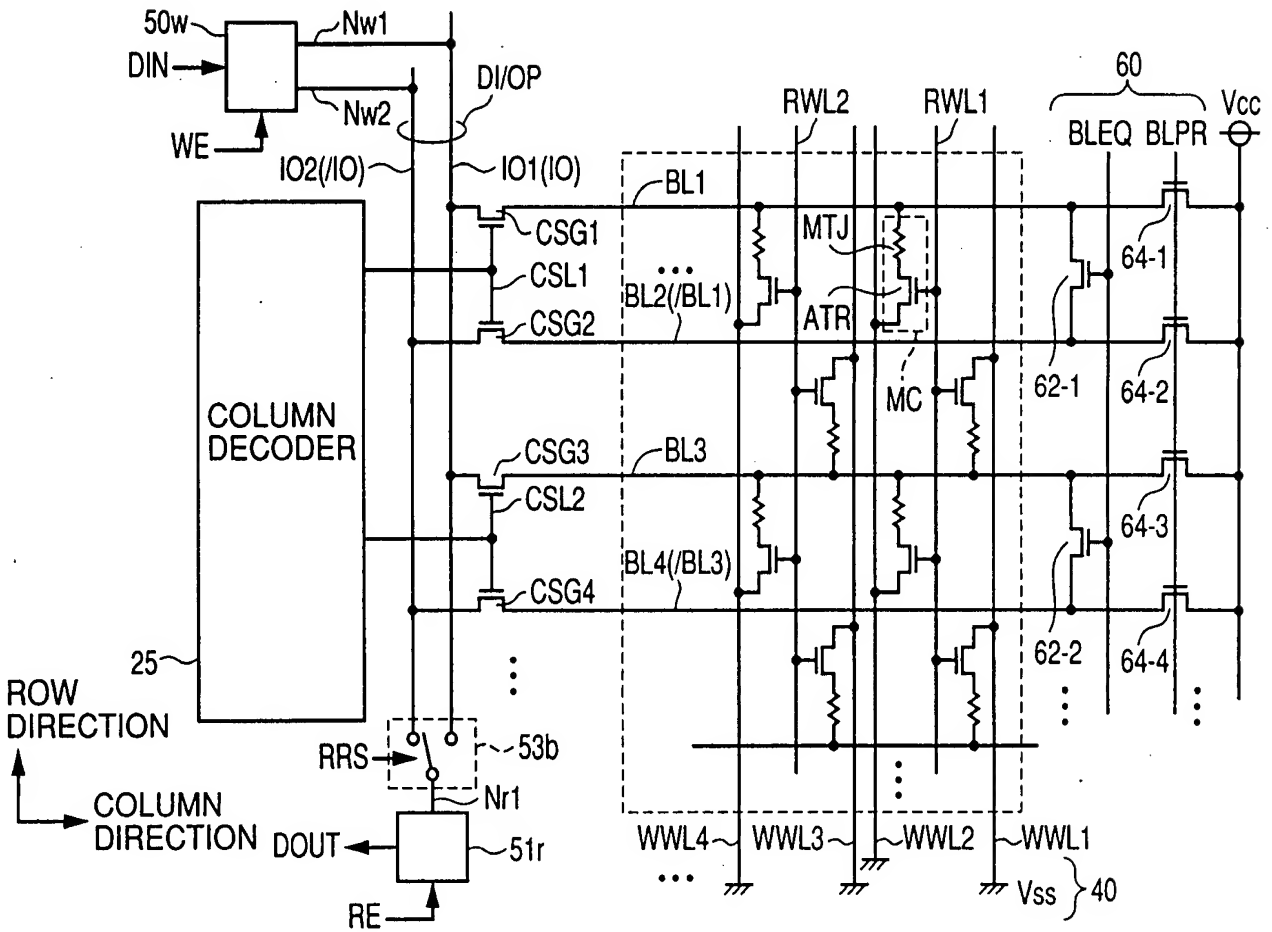
50w
Nw1
DIN
DI/OP
Nw2
WE
IO2(/IO)
IO1(IO)
BL1
CSG1
CSL1
CSG2
BL2(/BL1)
RWL2
RWL1
60
BLEQ
BLPR
Vcc
MTJ
ATR
MC
64-1
62-1
64-2
COLUMN DECODER
CSG3
BL3
CSL2
CSG4
BL4(/BL3)
64-3
62-2
64-4
25
ROW DIRECTION
RRS
53b
Nr1
COLUMN DIRECTION
DOUT
51r
RE
WWL4
WWL3
WWL2
WWL1
Vss
40

FIG.60

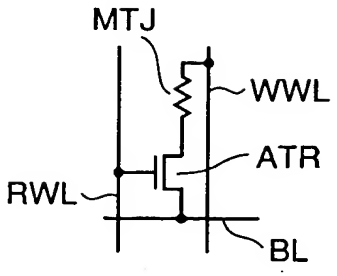
MTJ
WWL
ATR
RWL
BL

FIG.61

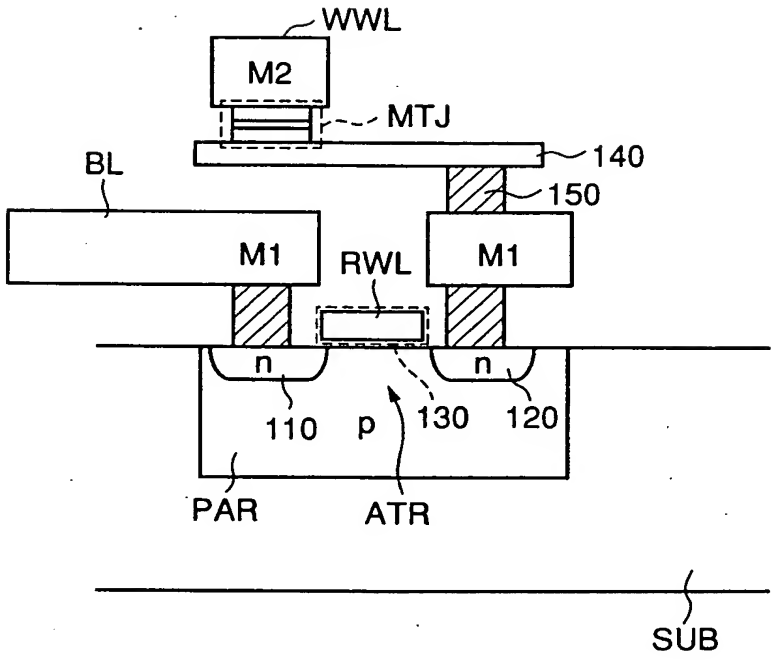
WWL
M2
MTJ
140
BL
150
M1
RWL
M1
n
n
110
p
130
120
PAR
ATR
SUB

FIG.62

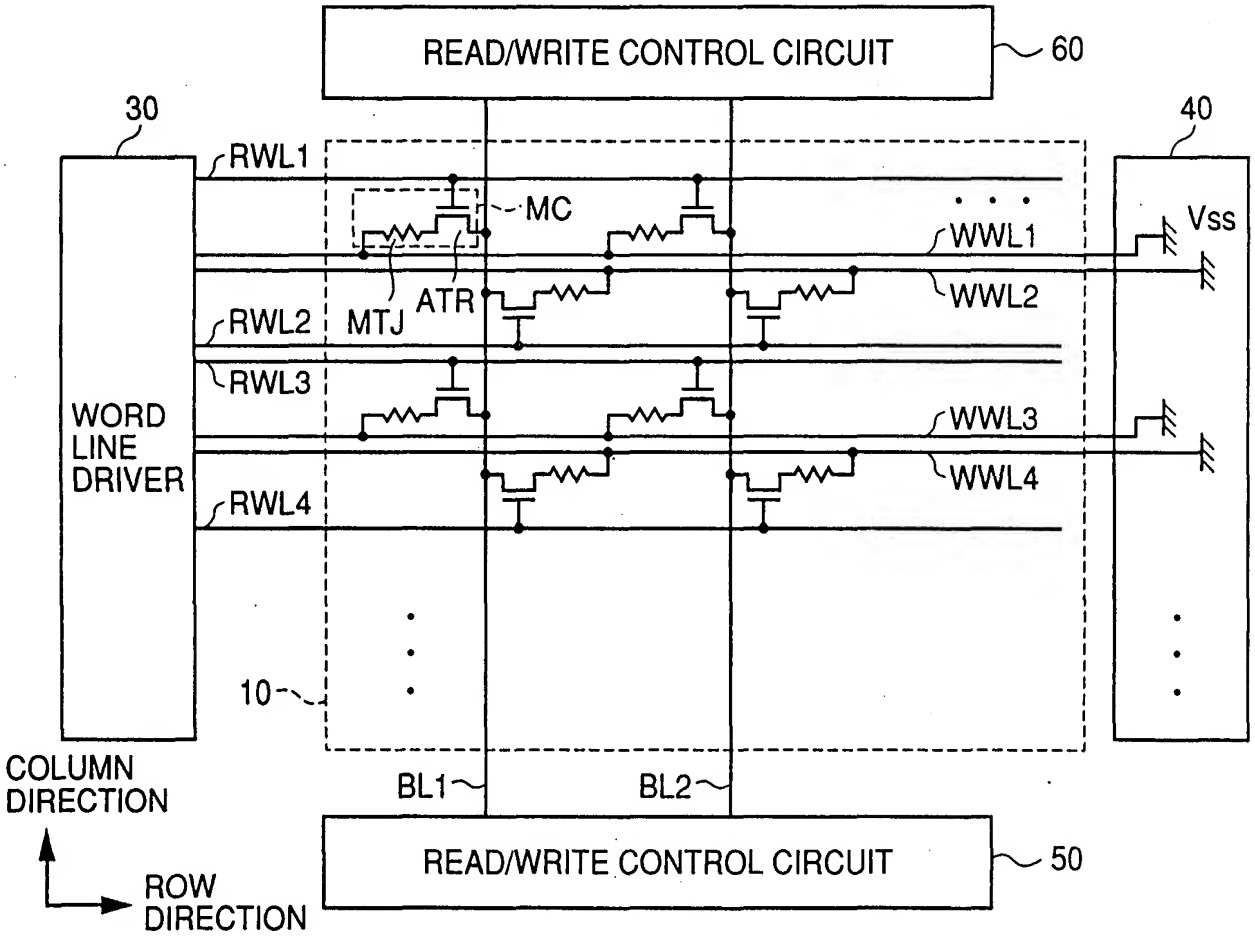
READ/WRITE CONTROL CIRCUIT
60
30
40
RWL1
MC
WWL1
Vss
MTJ
ATR
WWL2
RWL2
RWL3
WORD
LINE
DRIVER
WWL3
WWL4
RWL4
10
COLUMN
DIRECTION
BL1
BL2
READ/WRITE CONTROL CIRCUIT
50
ROW
DIRECTION

FIG.63

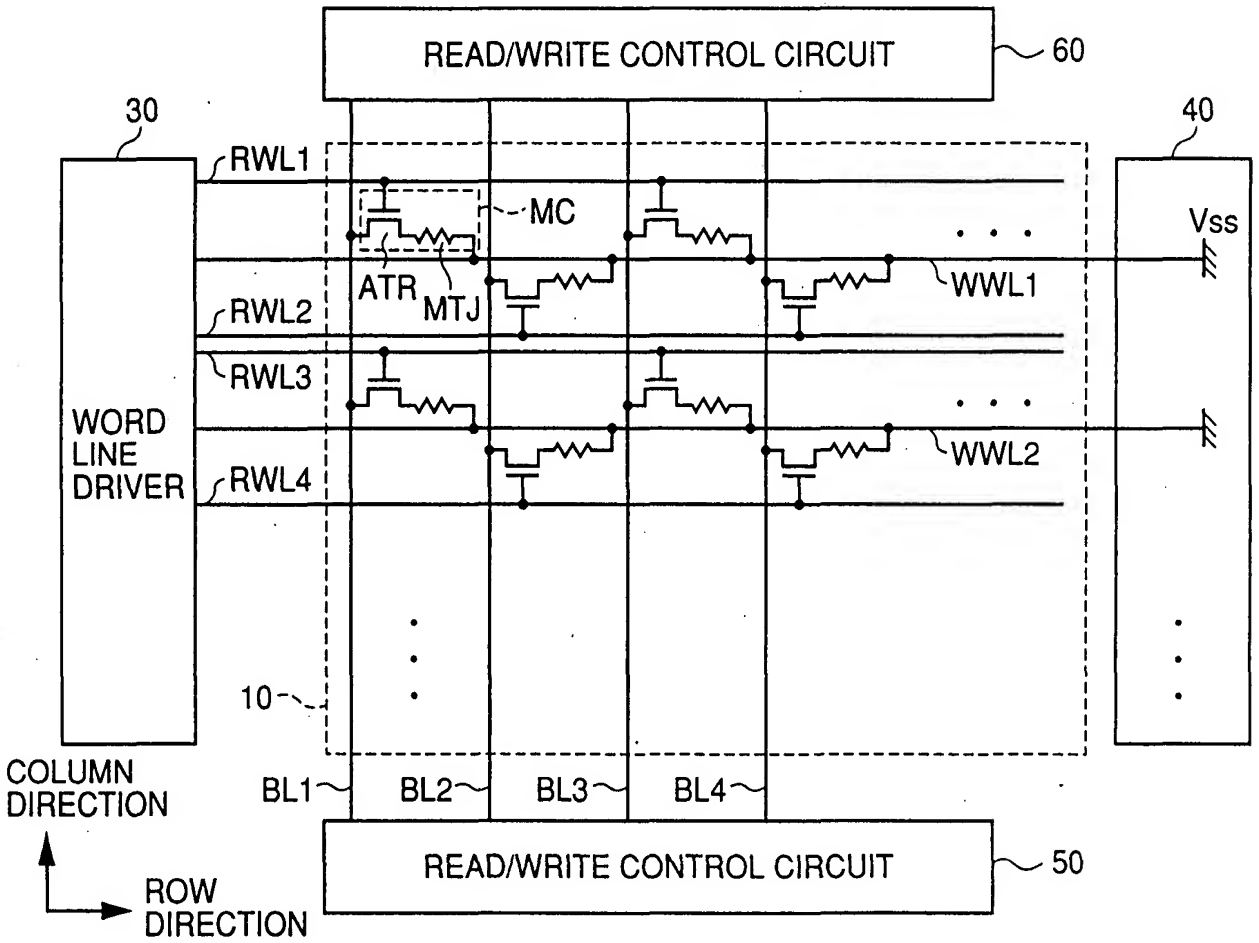
READ/WRITE CONTROL CIRCUIT
60
30
40
RWL1
MC
Vss
ATR
MTJ
WWL1
RWL2
RWL3
WORD
LINE
DRIVER
WWL2
RWL4
10
COLUMN
DIRECTION
BL1
BL2
BL3
BL4
READ/WRITE CONTROL CIRCUIT
50
ROW
DIRECTION

FIG.64

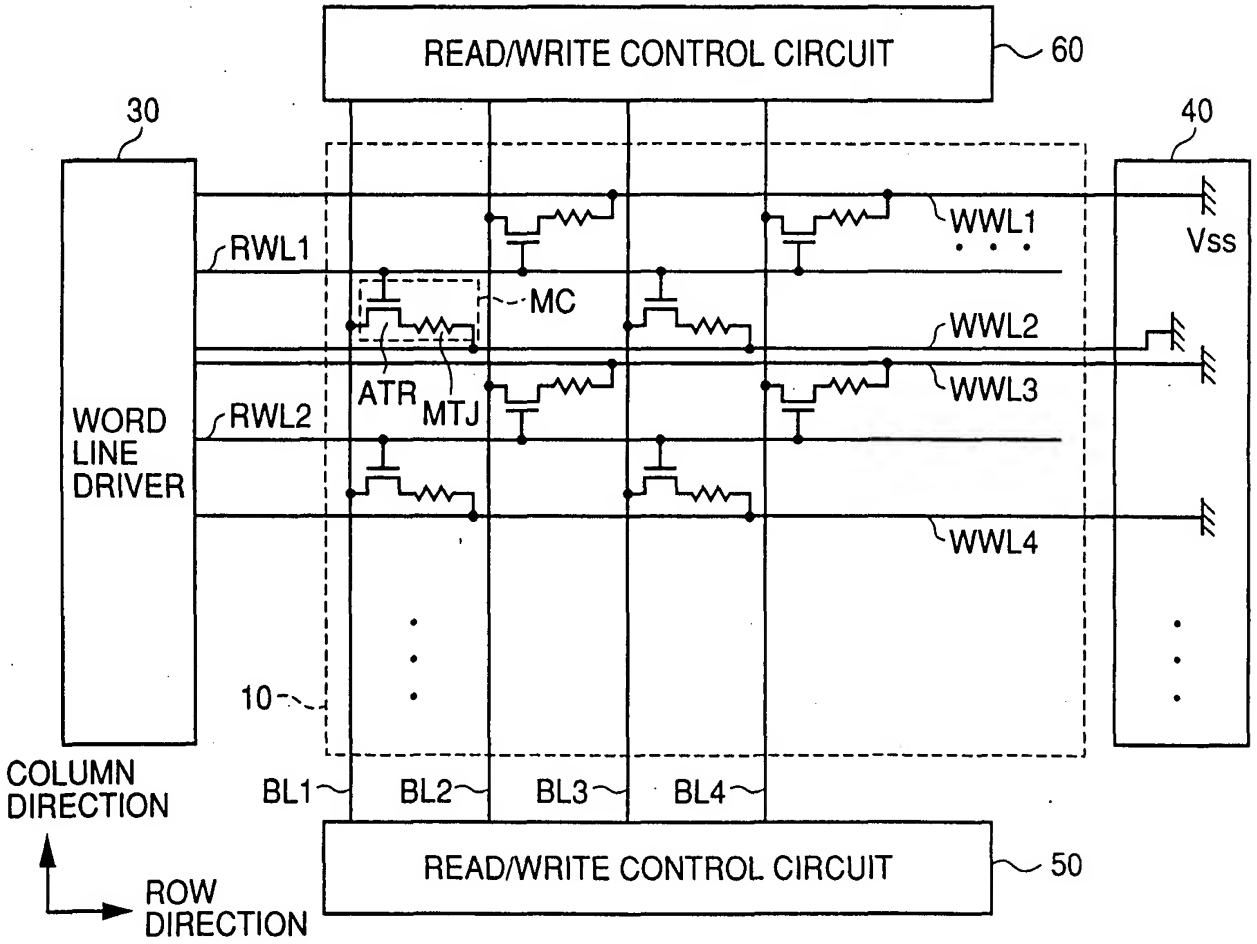
READ/WRITE CONTROL CIRCUIT
60
30
40
RWL1
RWL2
WORD
LINE
DRIVER
MC
ATR
MTJ
WWL1
WWL2
WWL3
WWL4
Vss
10
BL1
BL2
BL3
BL4
COLUMN
DIRECTION
ROW
DIRECTION
READ/WRITE CONTROL CIRCUIT
50

FIG.65

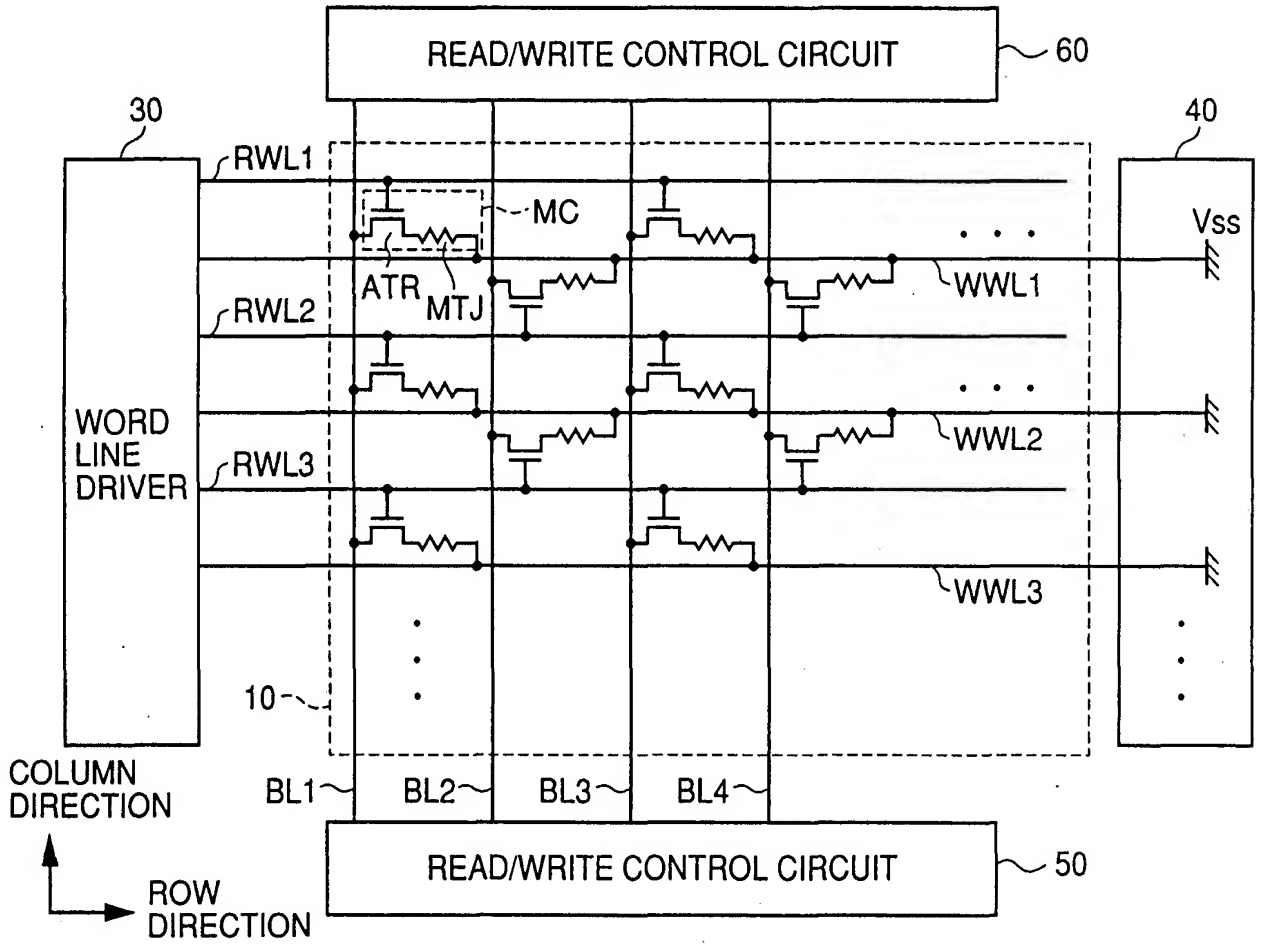
READ/WRITE CONTROL CIRCUIT
60
30
40
RWL1
MC
Vss
ATR
MTJ
WWL1
RWL2
WWL2
WORD LINE DRIVER
RWL3
WWL3
10
COLUMN DIRECTION
BL1
BL2
BL3
BL4
READ/WRITE CONTROL CIRCUIT
50
ROW DIRECTION

FIG.66

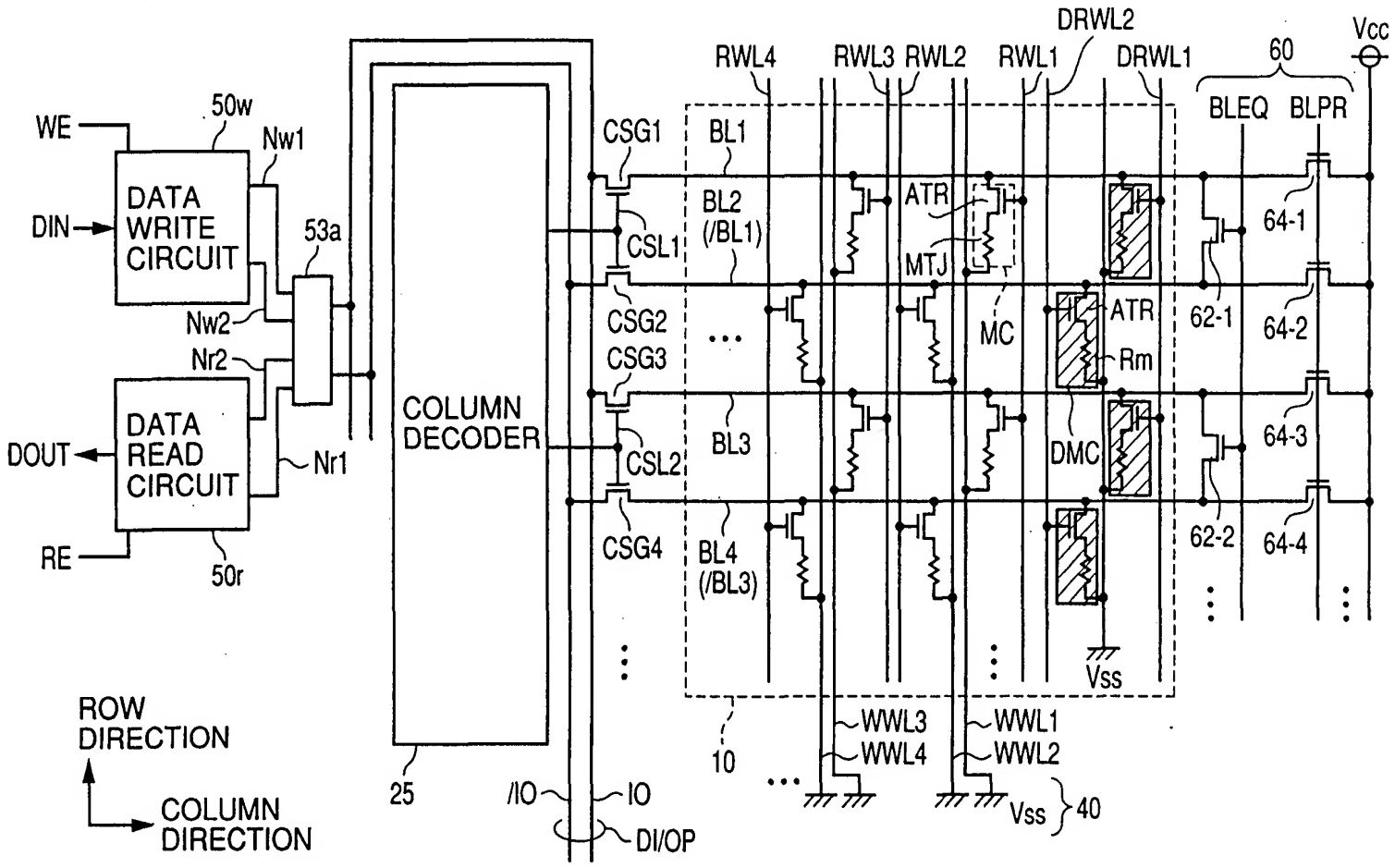
WE
50w
Nw1
DIN
DATA WRITE CIRCUIT
53a
Nw2
Nr2
DATA READ CIRCUIT
DOUT
Nr1
RE
50r
COLUMN DECODER
25
CSG1
CSL1
CSG2
CSG3
CSL2
CSG4
/IO
IO
DI/OP
RWL4
RWL3
RWL2
RWL1
DRWL2
DRWL1
60
BLEQ
BLPR
Vcc
BL1
BL2 (/BL1)
BL3
BL4 (/BL3)
ATR
MTJ
MC
DMC
Rm
62-1
62-2
64-1
64-2
64-3
64-4
Vss
10
WWL3
WWL4
WWL1
WWL2
Vss
40
ROW DIRECTION
COLUMN DIRECTION

FIG.67

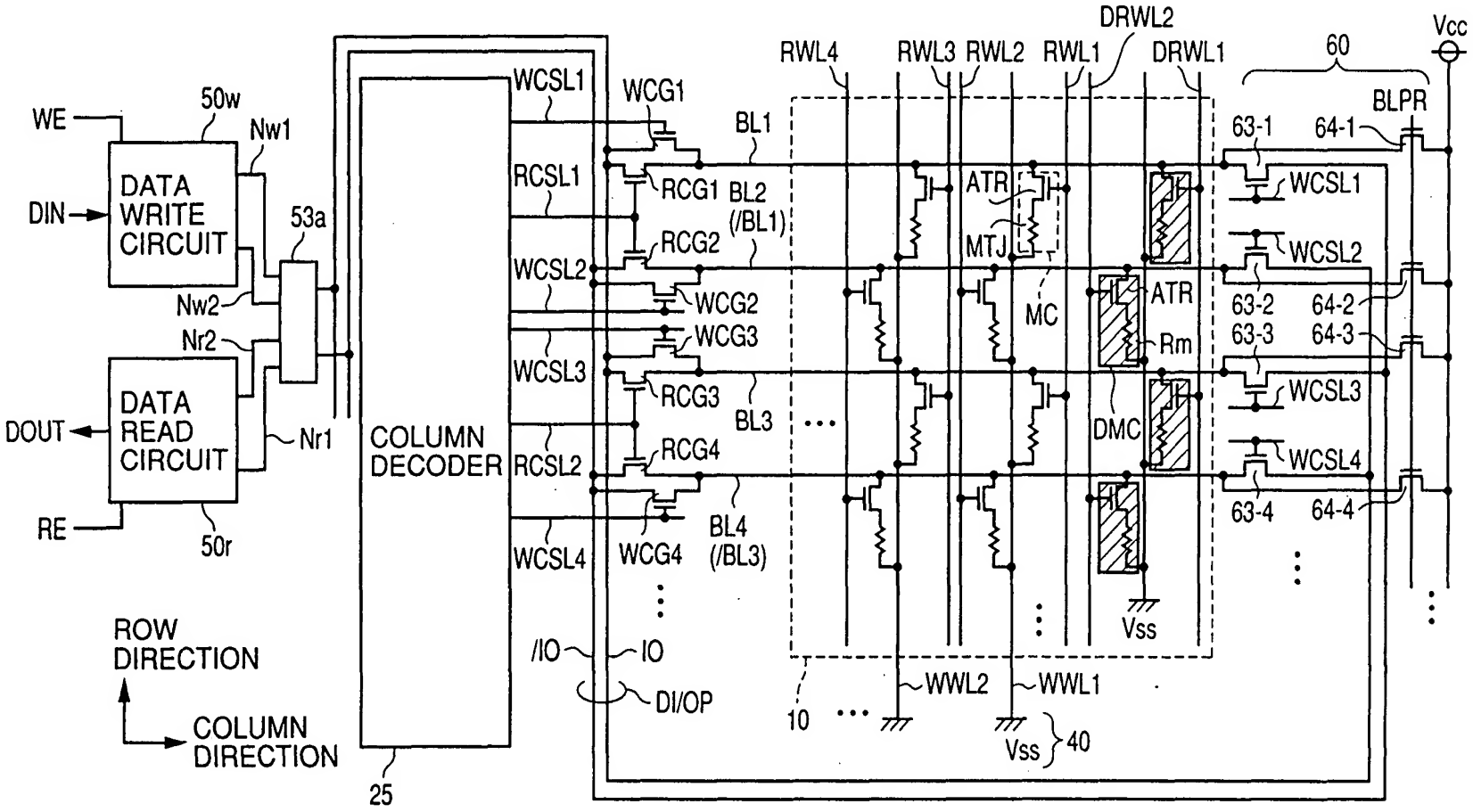
WE
50w
Nw1
DIN
DATA WRITE CIRCUIT
53a
Nw2
Nr2
DATA READ CIRCUIT
DOUT
Nr1
RE
50r
COLUMN DECODER
25
WCSL1
RCSL1
WCSL2
WCSL3
RCSL2
WCSL4
WCG1
RCG1
BL1
BL2 (/BL1)
RCG2
WCG2
WCG3
RCG3
BL3
RCG4
BL4 (/BL3)
WCG4
/IO
IO
DI/OP
ROW DIRECTION
COLUMN DIRECTION
RWL4
RWL3
RWL2
RWL1
DRWL2
DRWL1
60
Vcc
BLPR
63-1
64-1
ATR
MTJ
MC
Rm
DMC
WCSL1
WCSL2
63-2
64-2
63-3
64-3
WCSL3
WCSL4
63-4
64-4
Vss
WWL2
WWL1
10
Vss
40

FIG.68

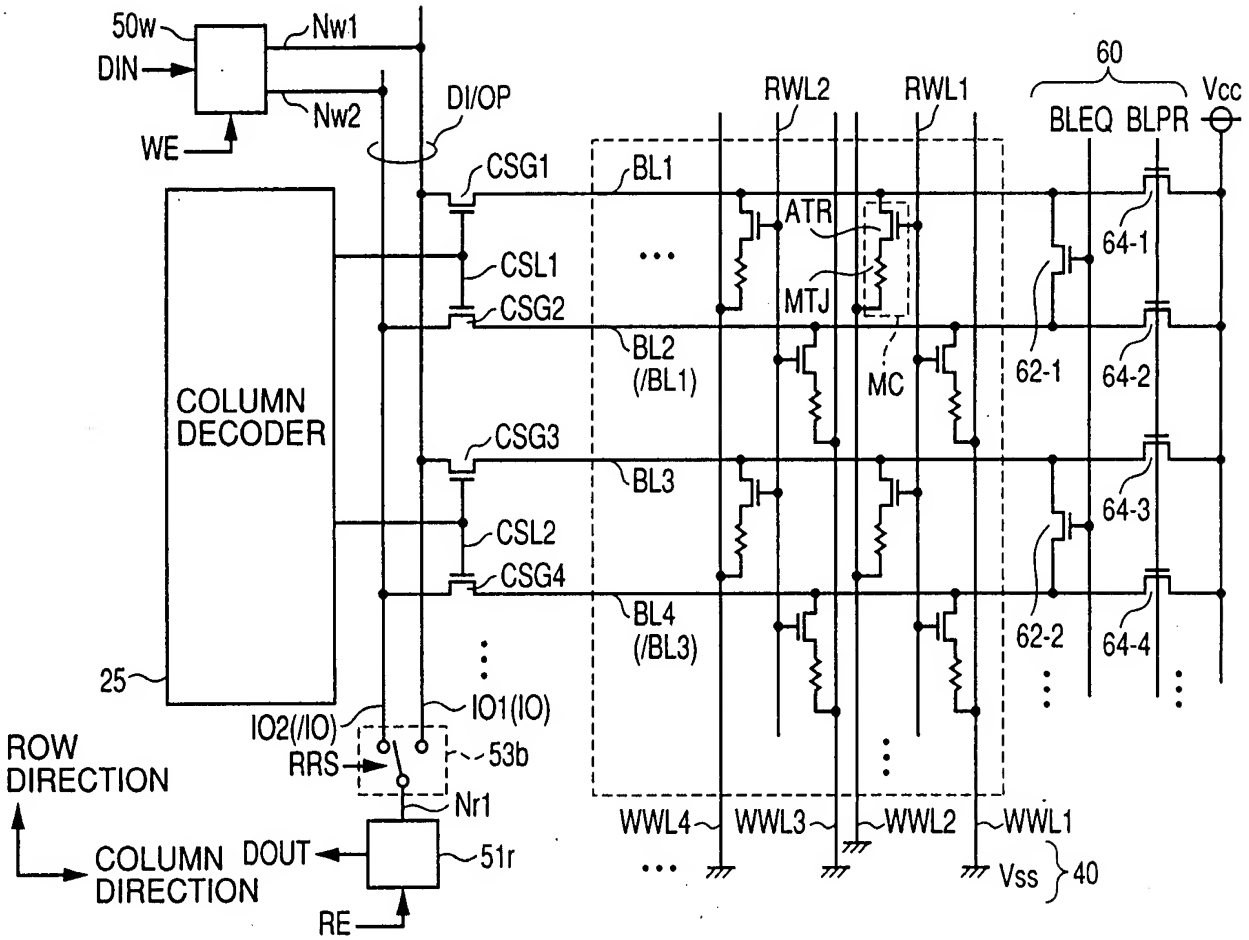
50w
DIN
WE
Nw1
Nw2
DI/OP
CSG1
CSL1
CSG2
CSG3
CSL2
CSG4
COLUMN DECODER
25
IO2(/IO)
IO1(IO)
RRS
53b
Nr1
51r
DOUT
RE
ROW DIRECTION
COLUMN DIRECTION
BL1
BL2 (/BL1)
BL3
BL4 (/BL3)
RWL2
RWL1
ATR
MTJ
MC
60
BLEQ
BLPR
Vcc
64-1
64-2
64-3
64-4
62-1
62-2
WWL4
WWL3
WWL2
WWL1
Vss
40

FIG.69

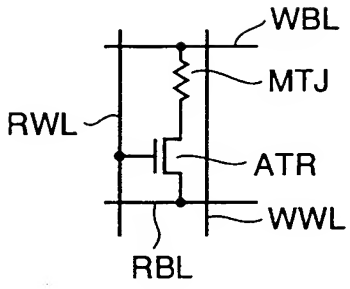
WBL
MTJ
RWL
ATR
WWL
RBL

FIG.70

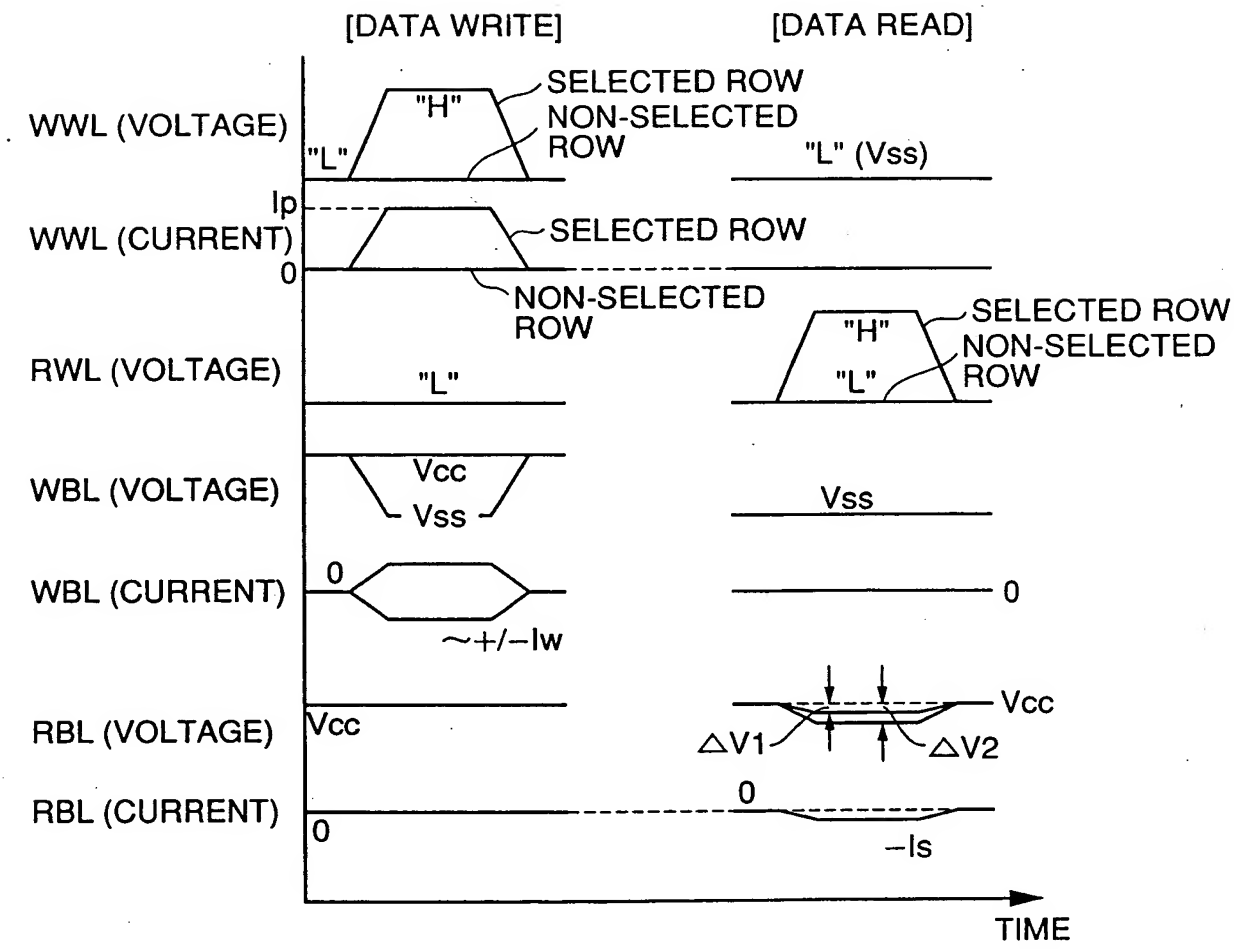
[DATA WRITE]
[DATA READ]
WWL (VOLTAGE)
"H"
"L"
SELECTED ROW
NON-SELECTED ROW
"L" (Vss)
Ip
WWL (CURRENT)
0
SELECTED ROW
NON-SELECTED ROW
RWL (VOLTAGE)
"L"
"H"
"L"
SELECTED ROW
NON-SELECTED ROW
WBL (VOLTAGE)
Vcc
Vss
Vss
WBL (CURRENT)
0
~+/−Iw
0
RBL (VOLTAGE)
Vcc
Vcc
△V1
△V2
RBL (CURRENT)
0
0
−Is
TIME

FIG.71

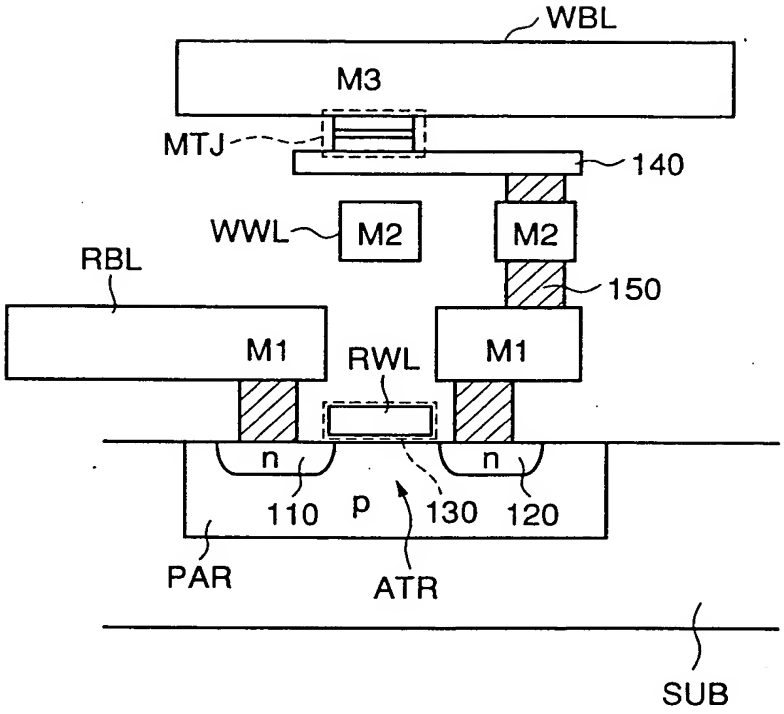
WBL
M3
MTJ
140
WWL
M2
M2
RBL
150
M1
RWL
M1
n
n
110
P
130
120
PAR
ATR
SUB

FIG.72

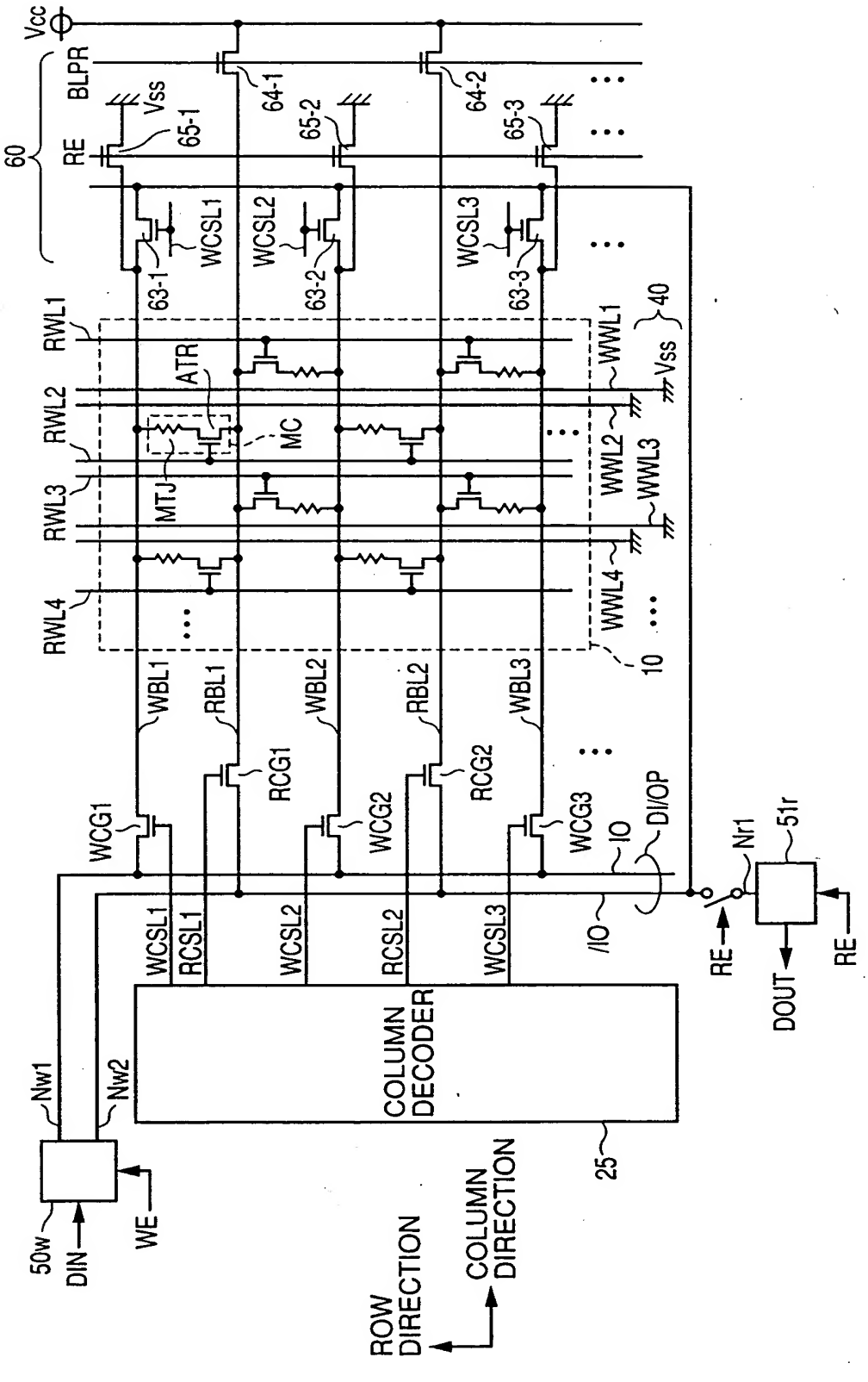
Vcc
BLPR
RE
Vss
60
65-1
64-1
65-2
64-2
65-3
WCSL1
WCSL2
WCSL3
63-1
63-2
63-3
RWL1
RWL2
RWL3
RWL4
ATR
MTJ
MC
WWL1
WWL2
WWL3
WWL4
40
10
Vss
WBL1
RBL1
WBL2
RBL2
WBL3
RCG1
RCG2
WCG1
WCG2
WCG3
IO
/IO
DI/OP
Nr1
51r
RE
DOUT
RE
WCSL1
RCSL1
WCSL2
RCSL2
WCSL3
COLUMN DECODER
25
Nw1
Nw2
50w
DIN
WE
ROW DIRECTION
COLUMN DIRECTION

FIG.73

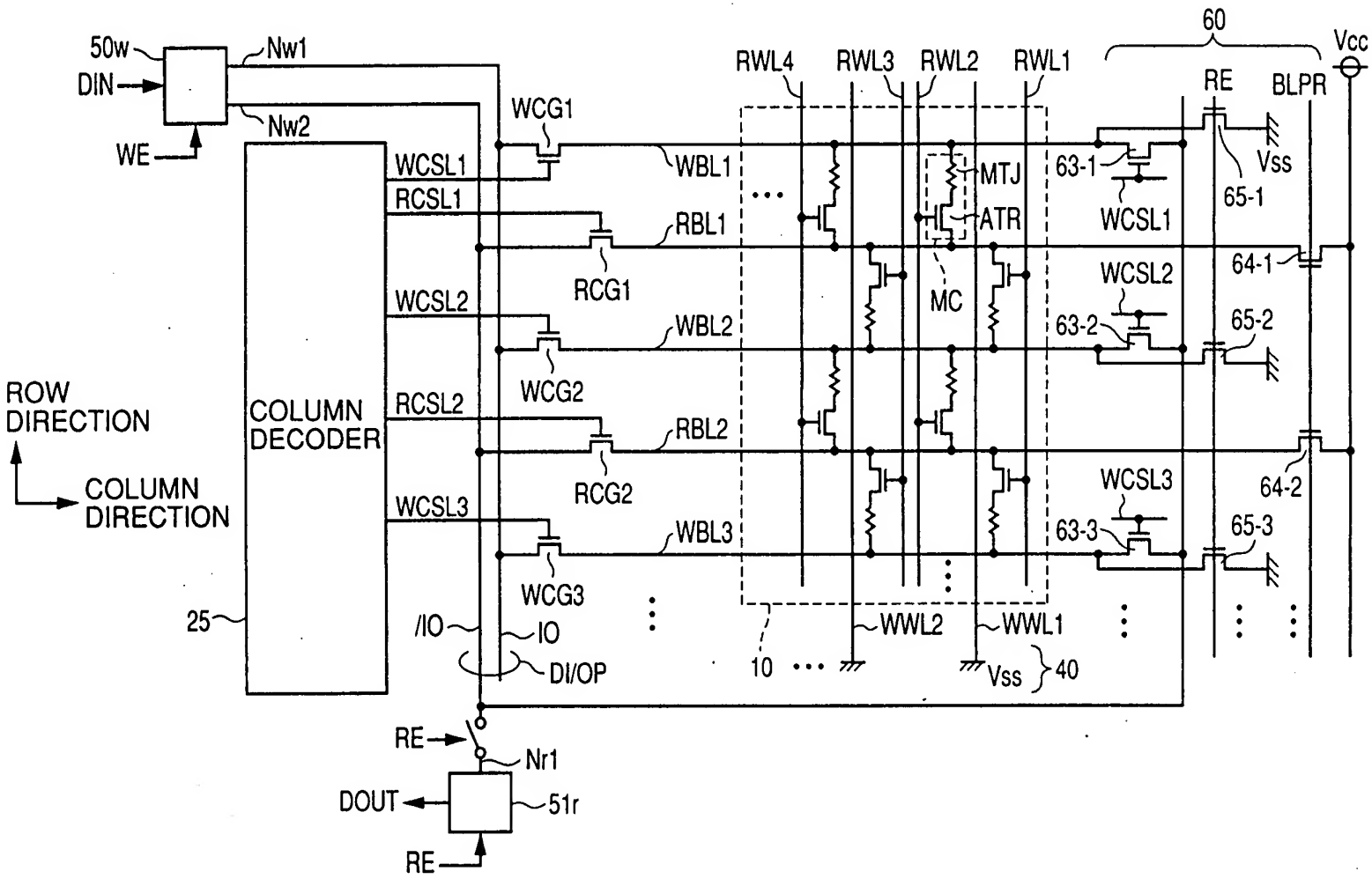
50w
DIN
WE
Nw1
Nw2
WCG1
WCSL1
RCSL1
WBL1
RBL1
RCG1
WCSL2
WBL2
WCG2
RCSL2
RBL2
RCG2
WCSL3
WBL3
WCG3
ROW DIRECTION
COLUMN DIRECTION
COLUMN DECODER
25
/IO
IO
DI/OP
RE
Nr1
DOUT
51r
RE
RWL4
RWL3
RWL2
RWL1
MTJ
ATR
MC
10
WWL2
WWL1
Vss
40
60
Vcc
RE
BLPR
63-1
WCSL1
65-1
Vss
64-1
WCSL2
63-2
65-2
64-2
WCSL3
63-3
65-3

FIG.74

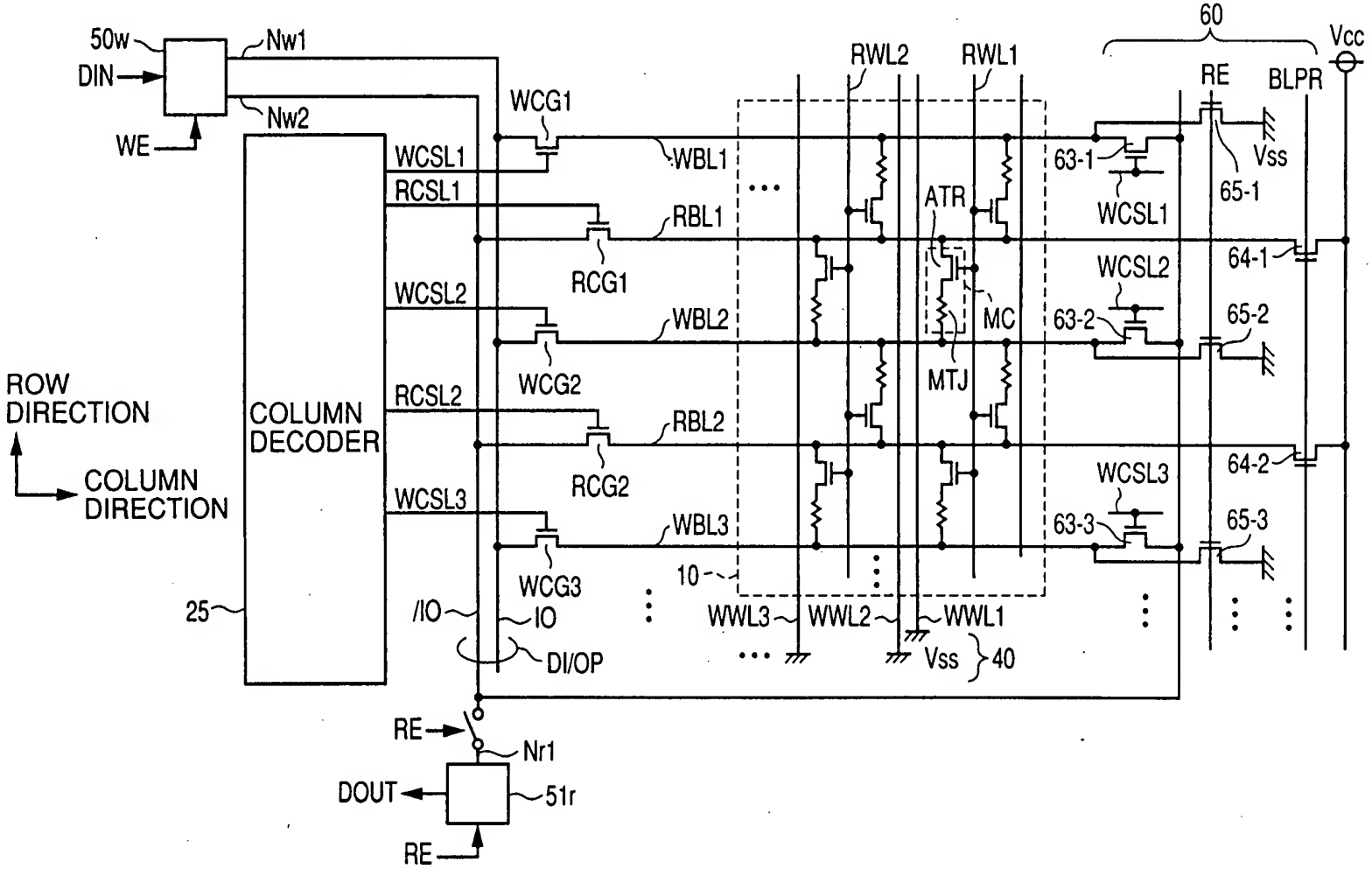
50w
DIN
WE
Nw1
Nw2
WCG1
WCSL1
RCSL1
WBL1
RBL1
RCG1
WCSL2
WBL2
WCG2
RCSL2
RBL2
RCG2
WCSL3
WBL3
WCG3
ROW DIRECTION
COLUMN DIRECTION
COLUMN DECODER
25
/IO
IO
DI/OP
10
RWL2
RWL1
ATR
MC
MTJ
WWL3
WWL2
WWL1
Vss
40
60
Vcc
RE
BLPR
63-1
WCSL1
65-1
64-1
WCSL2
63-2
65-2
64-2
WCSL3
63-3
65-3
RE
Nr1
DOUT
51r
RE

FIG.75

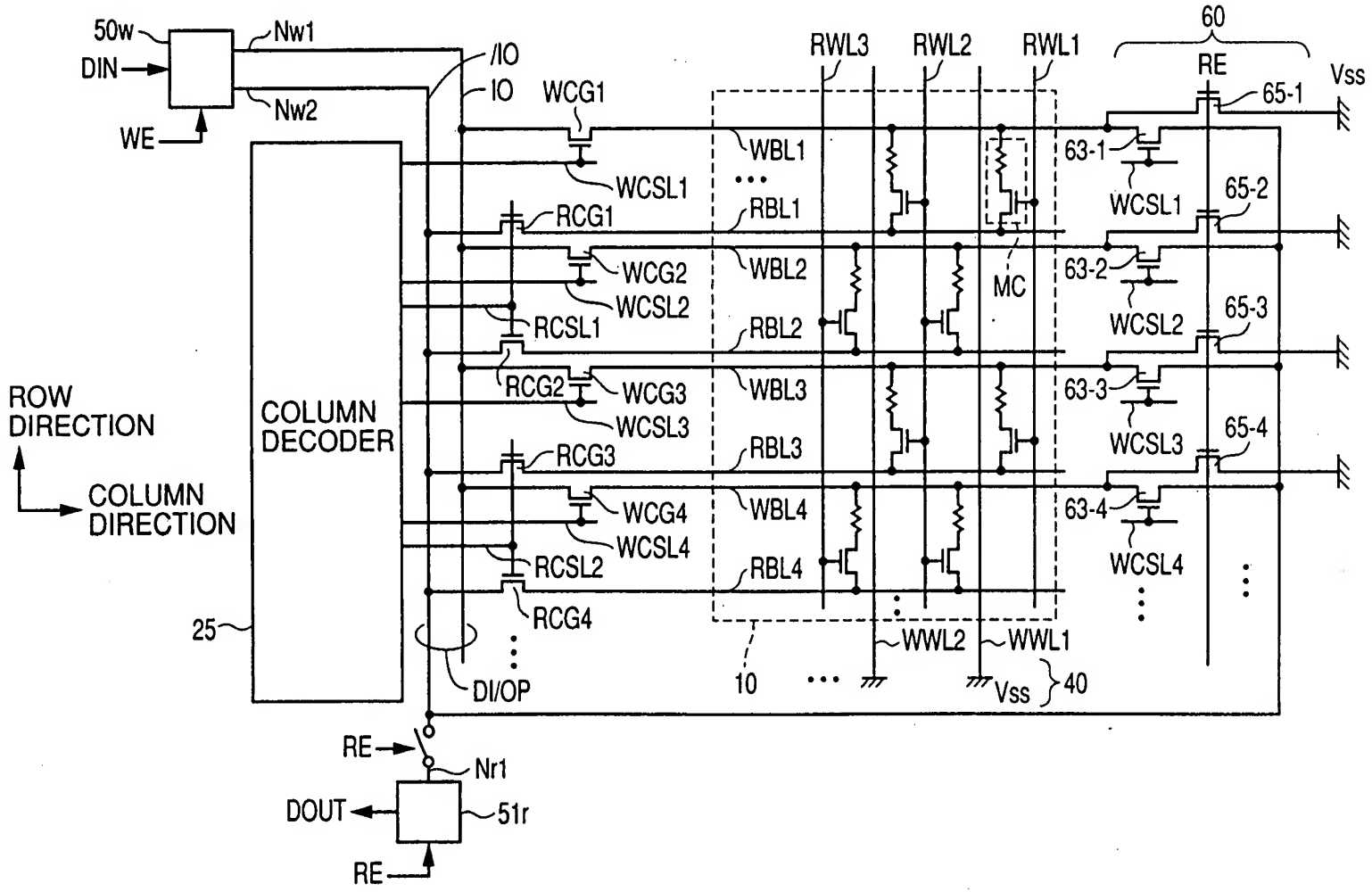
50w
DIN
WE
Nw1
Nw2
/IO
IO
WCG1
WCSL1
RCG1
WCG2
WCSL2
RCSL1
RCG2
WCG3
WCSL3
RCG3
WCG4
WCSL4
RCSL2
RCG4
DI/OP
25
COLUMN DECODER
ROW DIRECTION
COLUMN DIRECTION
RE
Nr1
DOUT
51r
RE
WBL1
RBL1
WBL2
RBL2
WBL3
RBL3
WBL4
RBL4
RWL3
RWL2
RWL1
MC
WWL2
WWL1
10
Vss
40
60
RE
65-1
Vss
63-1
WCSL1
65-2
63-2
WCSL2
65-3
63-3
WCSL3
65-4
63-4
WCSL4

FIG.76

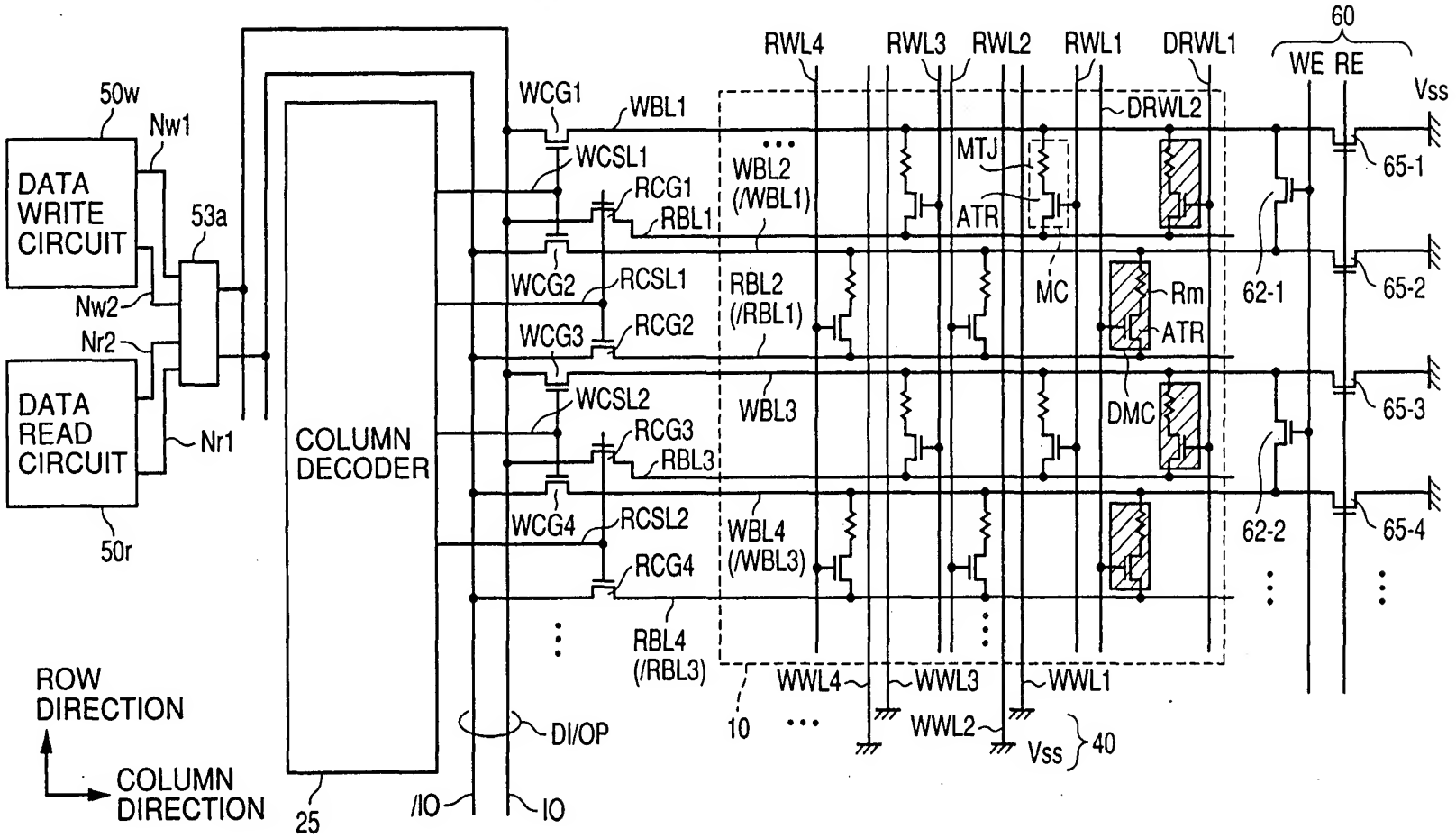
DATA WRITE CIRCUIT
DATA READ CIRCUIT
50w
50r
Nw1
Nw2
Nr2
Nr1
53a
COLUMN DECODER
25
ROW DIRECTION
COLUMN DIRECTION
WCG1
WCG2
WCG3
WCG4
WCSL1
WCSL2
RCSL1
RCSL2
RCG1
RCG2
RCG3
RCG4
WBL1
RBL1
WBL2 (/WBL1)
RBL2 (/RBL1)
WBL3
RBL3
WBL4 (/WBL3)
RBL4 (/RBL3)
RWL4
RWL3
RWL2
RWL1
DRWL1
DRWL2
MTJ
ATR
MC
Rm
DMC
60
WE RE
Vss
65-1
65-2
65-3
65-4
62-1
62-2
WWL4
WWL3
WWL2
WWL1
10
40
DI/OP
/IO
IO

FIG.77

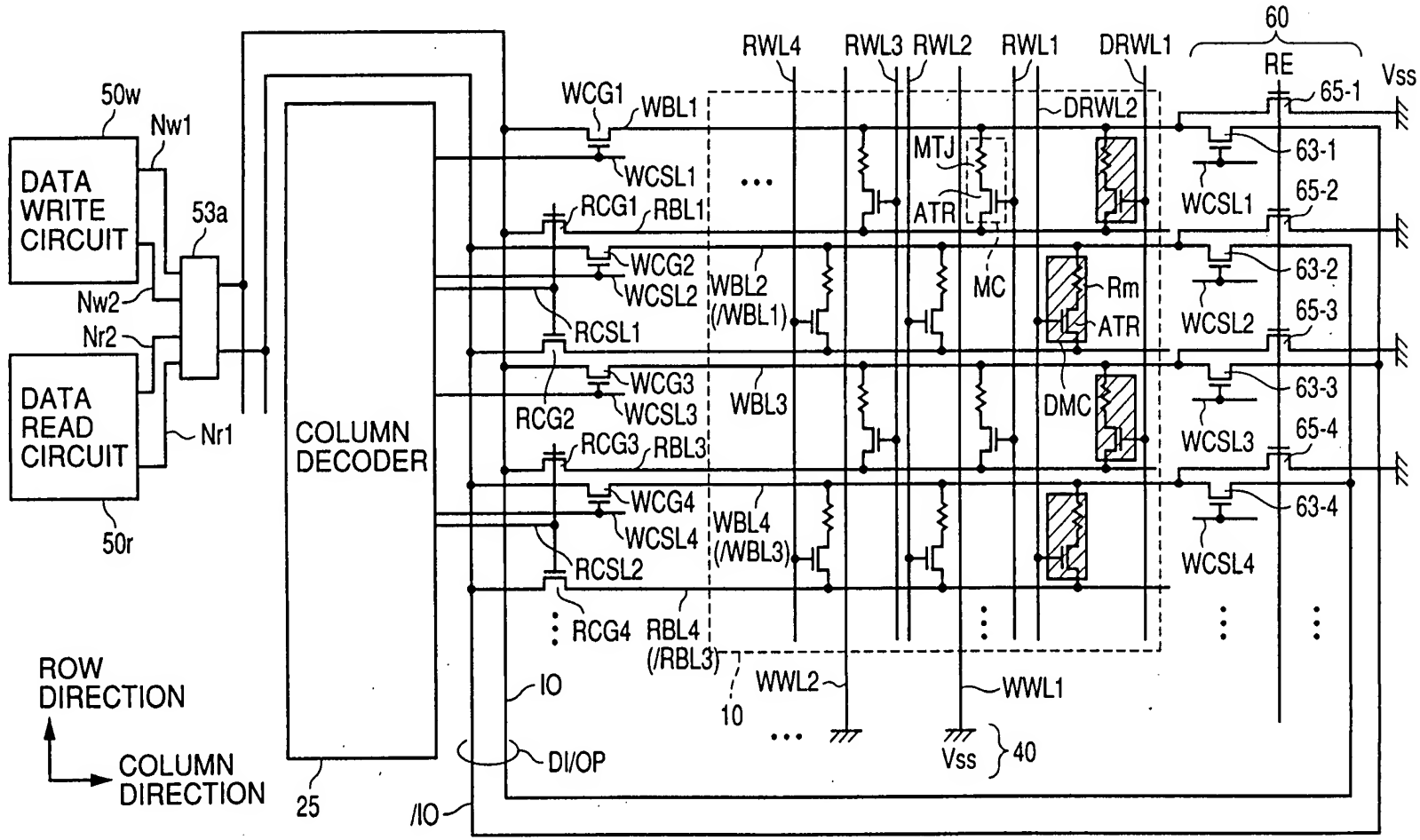
50w
Nw1
DATA WRITE CIRCUIT
53a
Nw2
Nr2
DATA READ CIRCUIT
Nr1
50r
COLUMN DECODER
25
ROW DIRECTION
COLUMN DIRECTION
WCG1
WBL1
WCSL1
RCG1
RBL1
WCG2
WCSL2
WBL2
(/WBL1)
RCSL1
WCG3
WCSL3
WBL3
RCG2
RCG3
RBL3
WCG4
WCSL4
WBL4
(/WBL3)
RCSL2
RCG4
RBL4
(/RBL3)
IO
/IO
DI/OP
10
RWL4
RWL3
RWL2
RWL1
DRWL1
DRWL2
MTJ
ATR
MC
Rm
ATR
DMC
WWL2
WWL1
Vss
40
60
RE
65-1
Vss
63-1
WCSL1
65-2
63-2
WCSL2
65-3
63-3
WCSL3
65-4
63-4
WCSL4

FIG.78

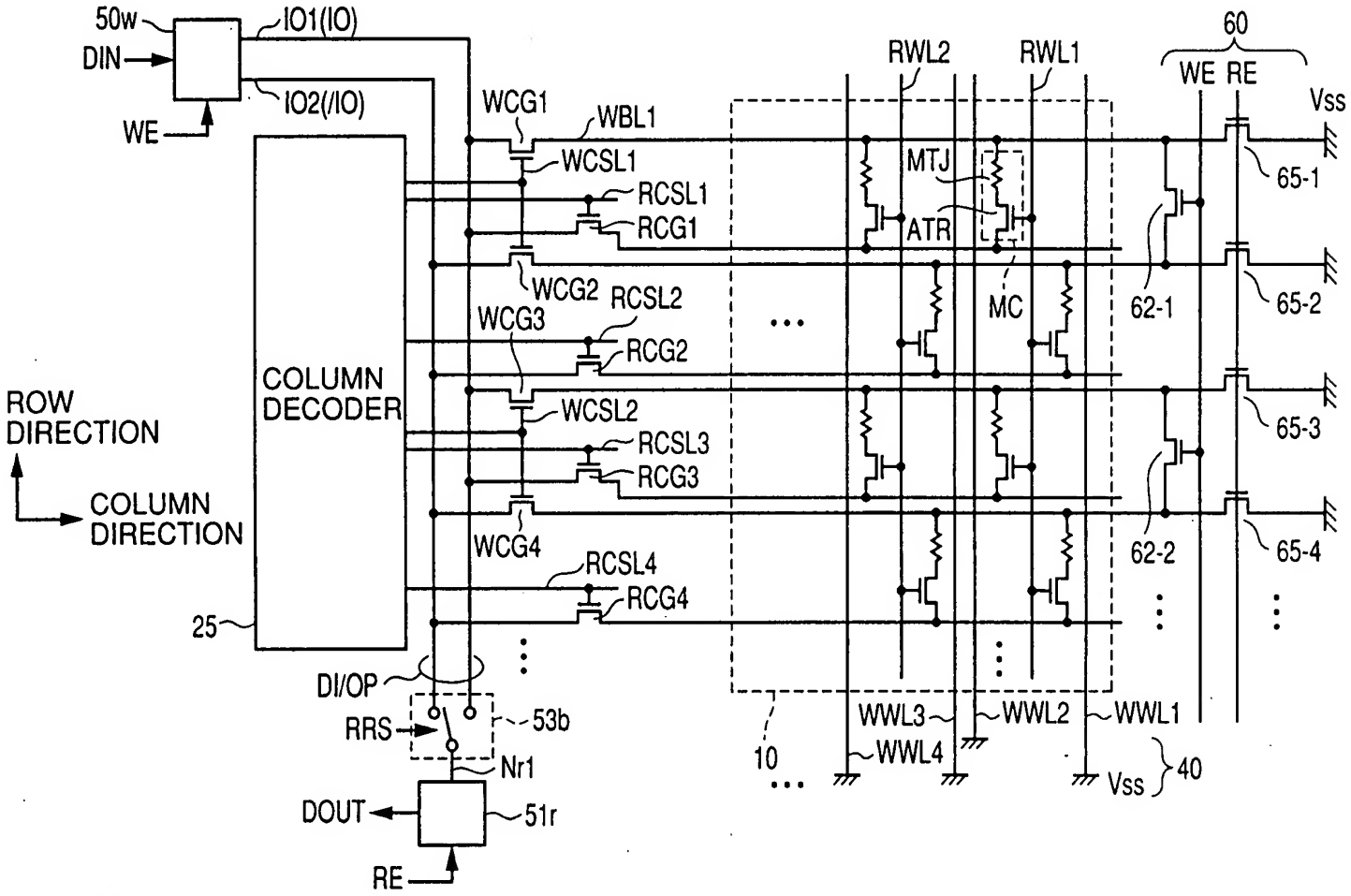
50w
DIN
WE
IO1(IO)
IO2(/IO)
WCG1
WBL1
WCSL1
RCSL1
RCG1
WCG2
RCSL2
WCG3
RCG2
WCSL2
RCSL3
RCG3
WCG4
RCSL4
RCG4
COLUMN DECODER
25
ROW DIRECTION
COLUMN DIRECTION
DI/OP
RRS
53b
Nr1
DOUT
51r
RE
RWL2
RWL1
MTJ
ATR
MC
10
WWL3
WWL4
WWL2
WWL1
Vss
40
60
WE RE
Vss
65-1
65-2
65-3
65-4
62-1
62-2

FIG.79

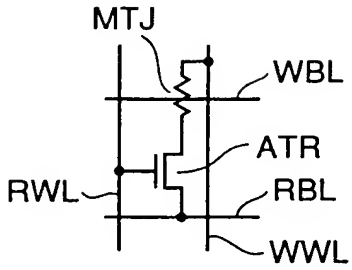
MTJ
WBL
ATR
RWL
RBL
WWL

FIG.80

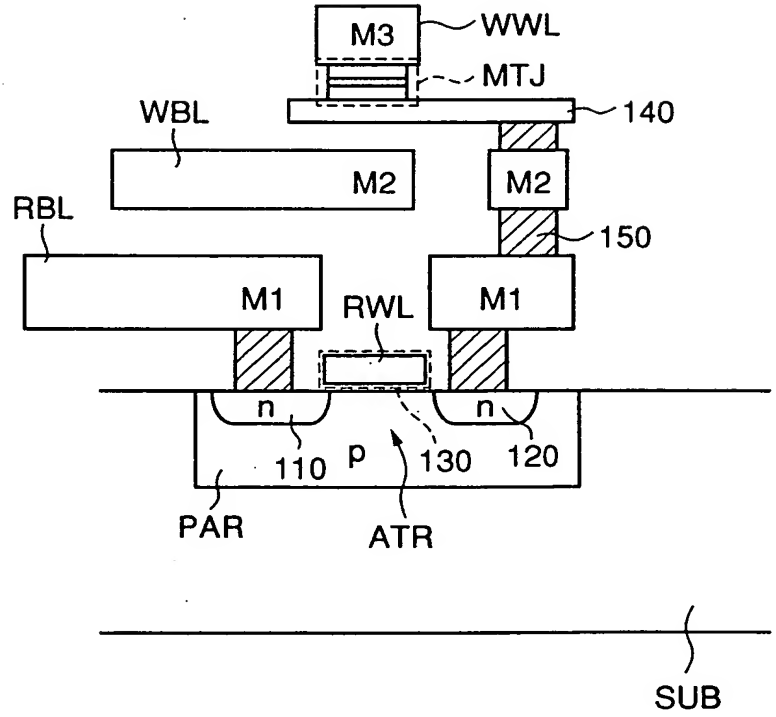
M3
WWL
MTJ
WBL
140
M2
M2
RBL
150
M1
RWL
M1
n
n
110
p
130
120
PAR
ATR
SUB

FIG.81

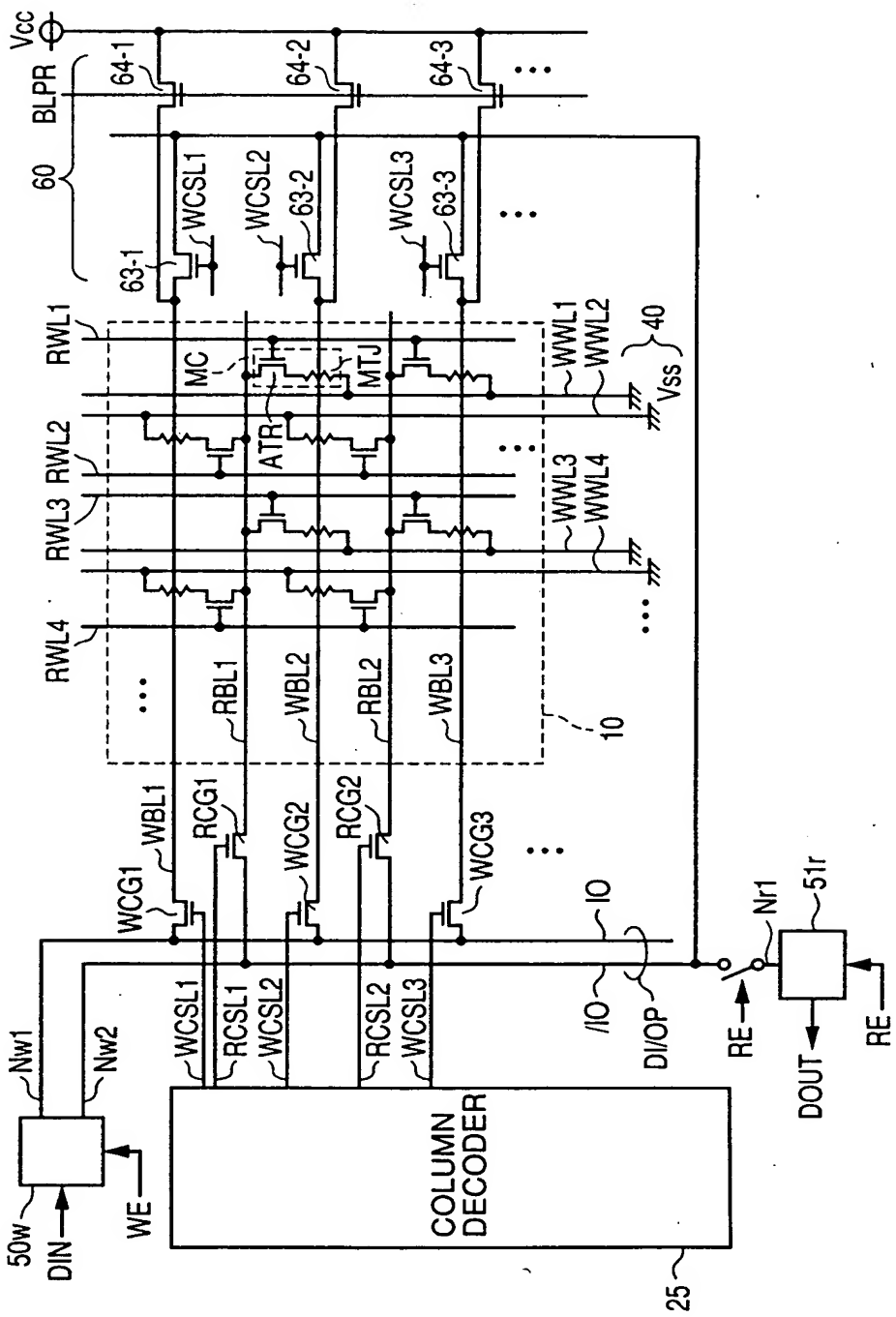
Vcc
BLPR
60
64-1
64-2
64-3
63-1
63-2
63-3
WCSL1
WCSL2
WCSL3
RWL1
RWL2
RWL3
RWL4
MC
ATR
MTJ
WWL1
WWL2
WWL3
WWL4
40
Vss
10
RBL1
RBL2
WBL1
WBL2
WBL3
WCG1
WCG2
WCG3
RCG1
RCG2
IO
/IO
DI/OP
Nr1
51r
RE
DOUT
Nw1
Nw2
RCSL1
RCSL2
50w
DIN
WE
COLUMN DECODER
25

FIG.82

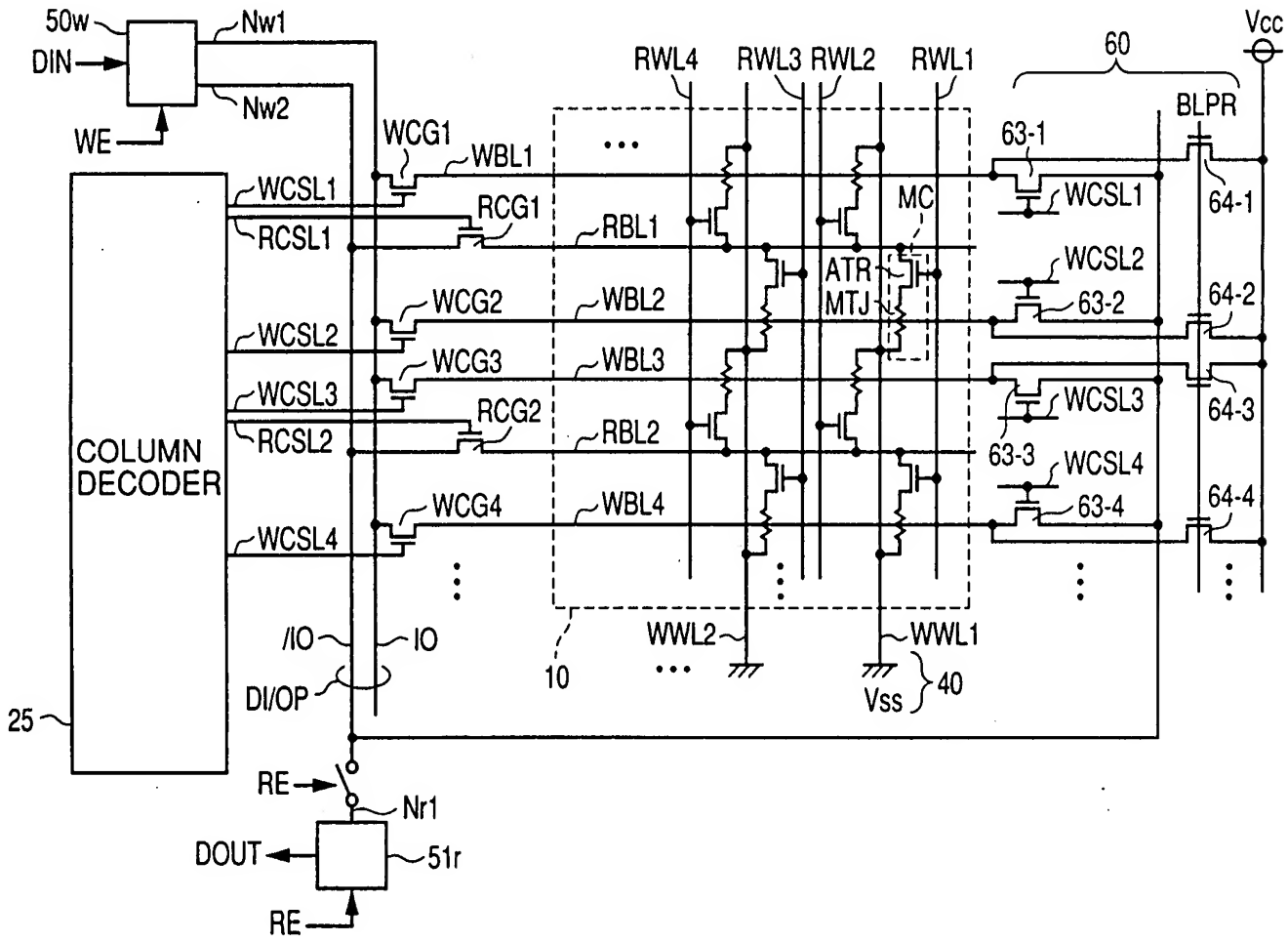
50w
DIN
WE
Nw1
Nw2
COLUMN DECODER
25
WCSL1
RCSL1
WCSL2
WCSL3
RCSL2
WCSL4
WCG1
WBL1
RCG1
RBL1
WCG2
WBL2
WCG3
WBL3
RCG2
RBL2
WCG4
WBL4
/IO
IO
DI/OP
10
RWL4
RWL3
RWL2
RWL1
MC
ATR
MTJ
WWL2
WWL1
Vss
40
60
Vcc
BLPR
63-1
63-2
63-3
63-4
64-1
64-2
64-3
64-4
RE
Nr1
DOUT
51r
RE

FIG.83

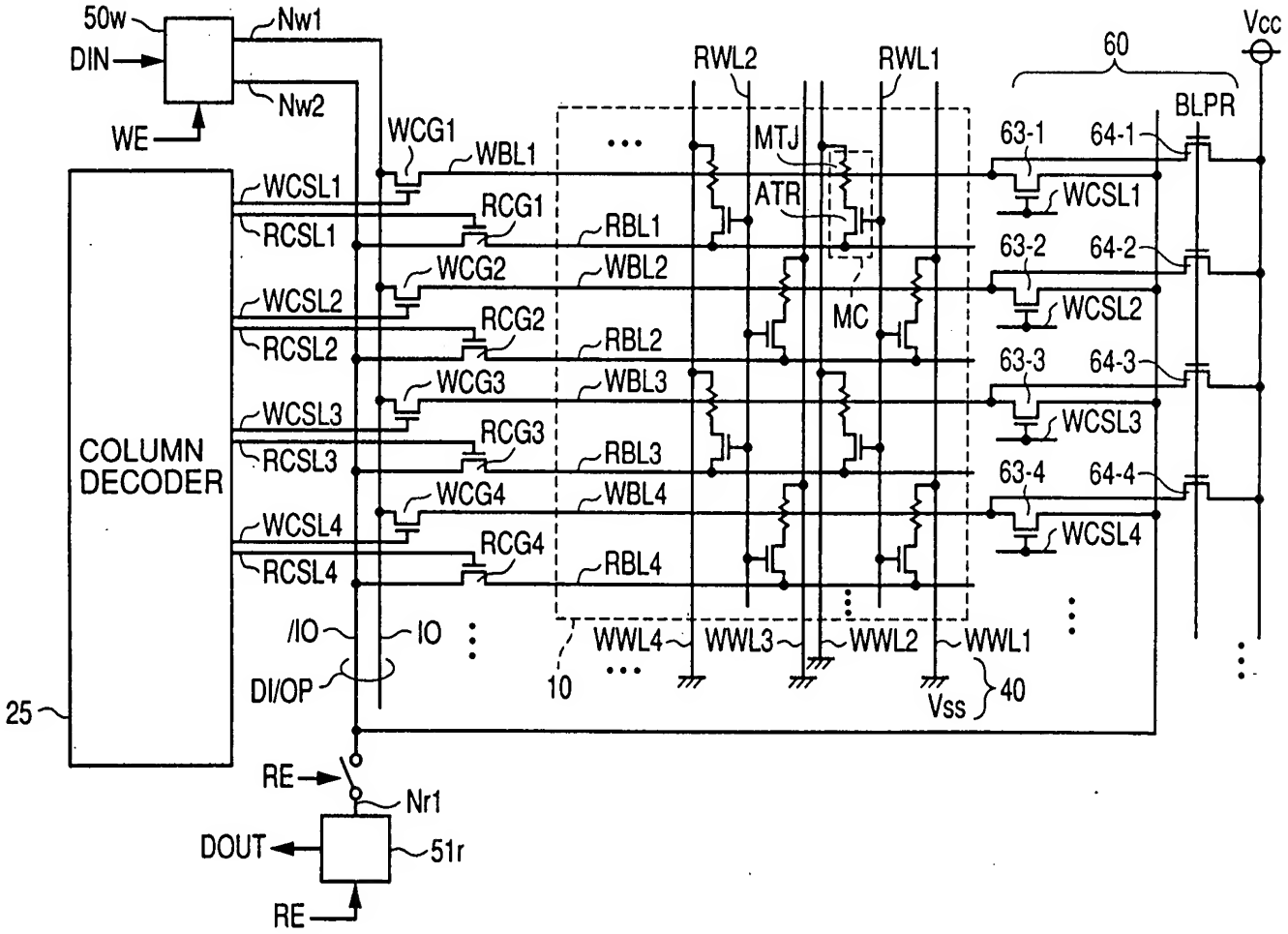
50w
DIN
WE
Nw1
Nw2
WCG1
WBL1
WCSL1
RCG1
RCSL1
RBL1
WCG2
WBL2
WCSL2
RCG2
RCSL2
RBL2
WCG3
WBL3
WCSL3
RCG3
RCSL3
RBL3
WCG4
WBL4
WCSL4
RCG4
RCSL4
RBL4
COLUMN DECODER
25
/IO
IO
DI/OP
10
RWL2
RWL1
MTJ
ATR
MC
WWL4
WWL3
WWL2
WWL1
Vss
40
60
Vcc
BLPR
63-1
64-1
63-2
64-2
63-3
64-3
63-4
64-4
RE
Nr1
DOUT
51r
RE

FIG.84

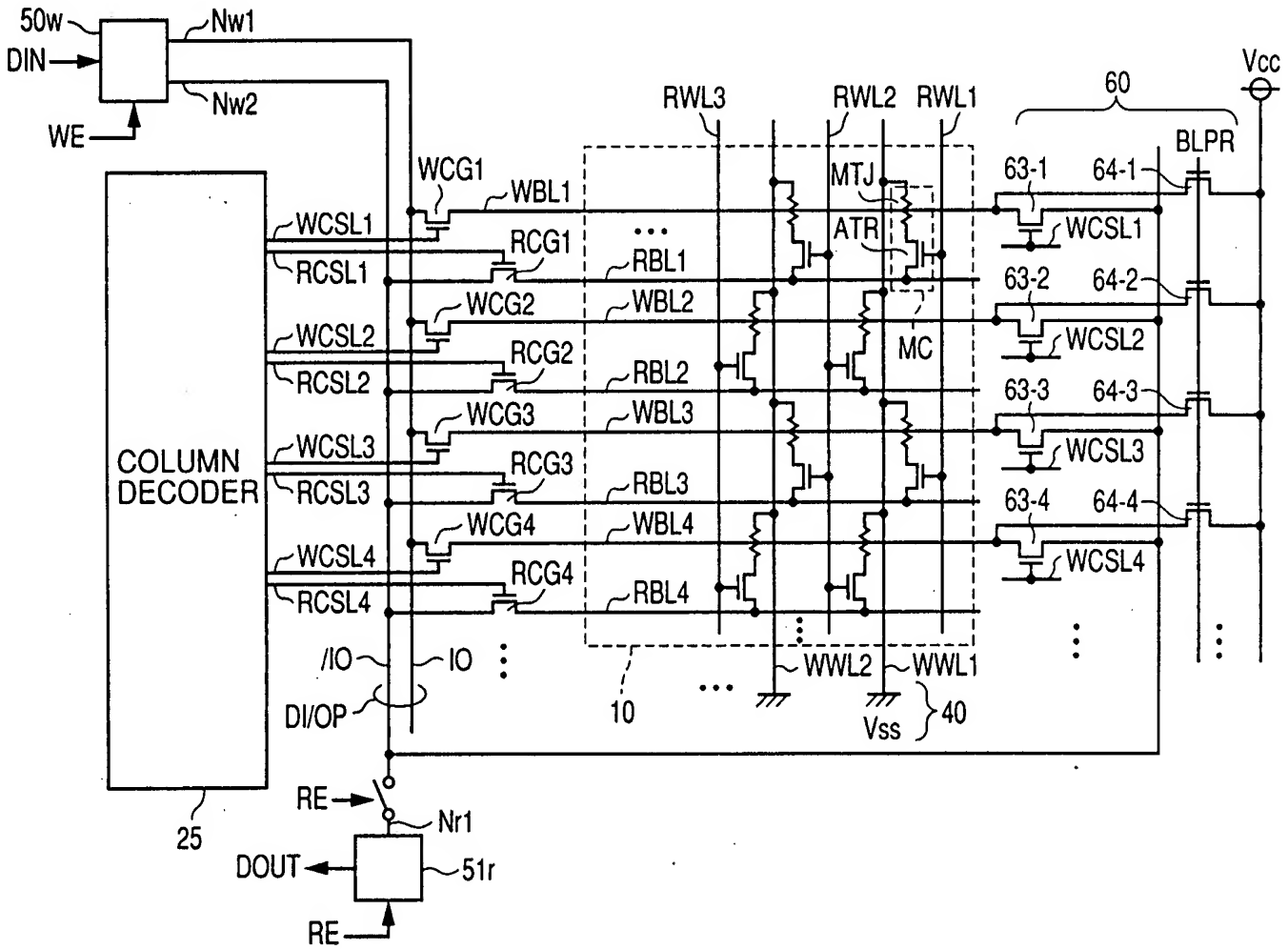
50w
DIN
WE
Nw1
Nw2
COLUMN DECODER
25
WCG1
WBL1
WCSL1
RCG1
RCSL1
RBL1
WCG2
WBL2
WCSL2
RCG2
RCSL2
RBL2
WCG3
WBL3
WCSL3
RCG3
RCSL3
RBL3
WCG4
WBL4
WCSL4
RCG4
RCSL4
RBL4
/IO
IO
DI/OP
RE
Nr1
DOUT
51r
RE
RWL3
RWL2
RWL1
MTJ
ATR
MC
10
WWL2
WWL1
Vss
40
60
Vcc
BLPR
63-1
64-1
63-2
64-2
63-3
64-3
63-4
64-4
WCSL1
WCSL2
WCSL3
WCSL4

FIG.85

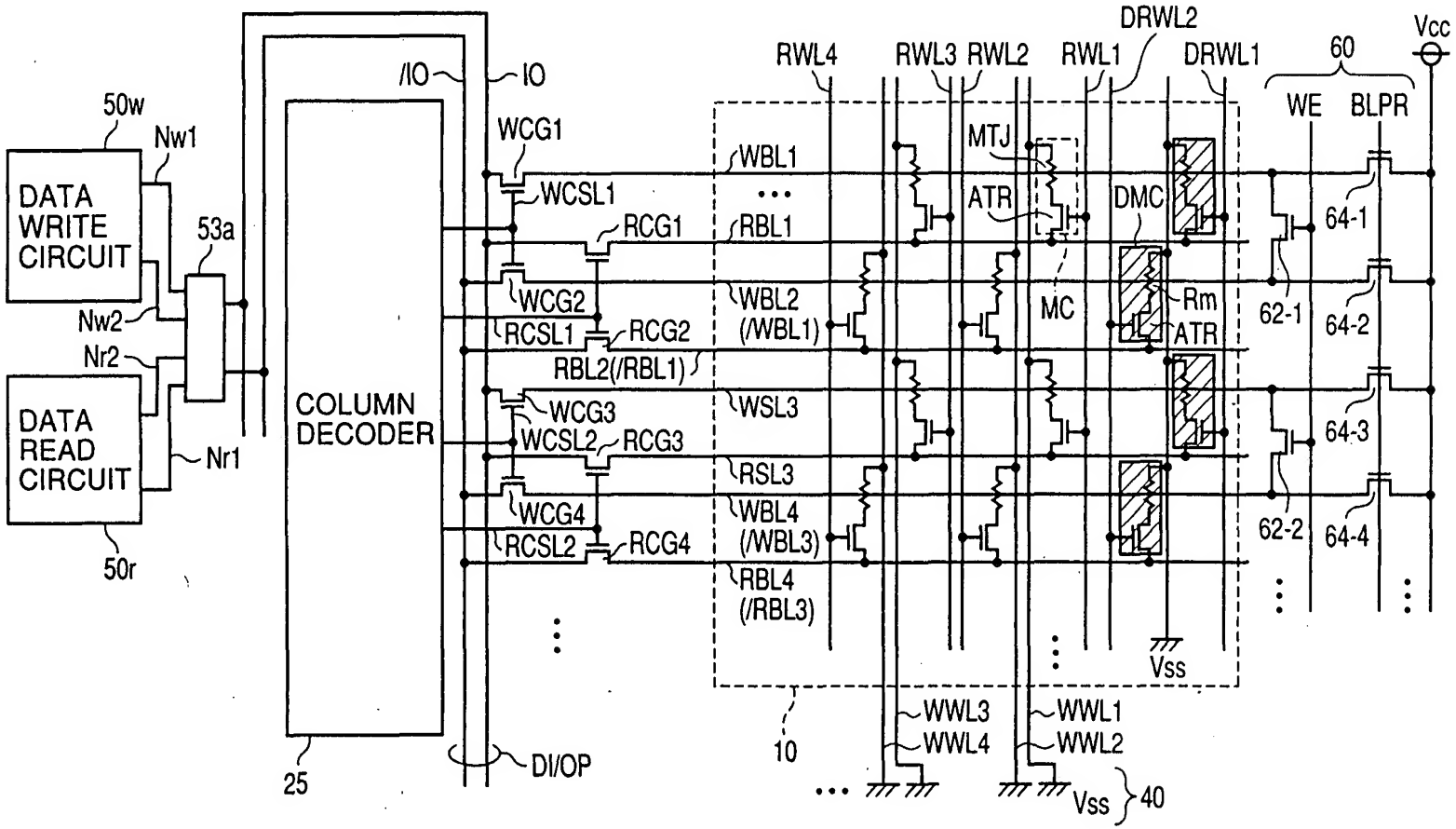
50w
Nw1
DATA WRITE CIRCUIT
53a
Nw2
Nr2
DATA READ CIRCUIT
Nr1
50r
COLUMN DECODER
25
/IO
IO
WCG1
WCSL1
RCG1
WCG2
RCSL1
RCG2
RBL2(/RBL1)
WCG3
WCSL2
RCG3
WCG4
RCSL2
RCG4
DI/OP
RWL4
RWL3
RWL2
RWL1
DRWL2
DRWL1
60
Vcc
WE
BLPR
WBL1
RBL1
WBL2 (/WBL1)
WSL3
RSL3
WBL4 (/WBL3)
RBL4 (/RBL3)
MTJ
ATR
DMC
MC
Rm
ATR
64-1
64-2
64-3
64-4
62-1
62-2
Vss
10
WWL3
WWL4
WWL1
WWL2
Vss
40

FIG.86

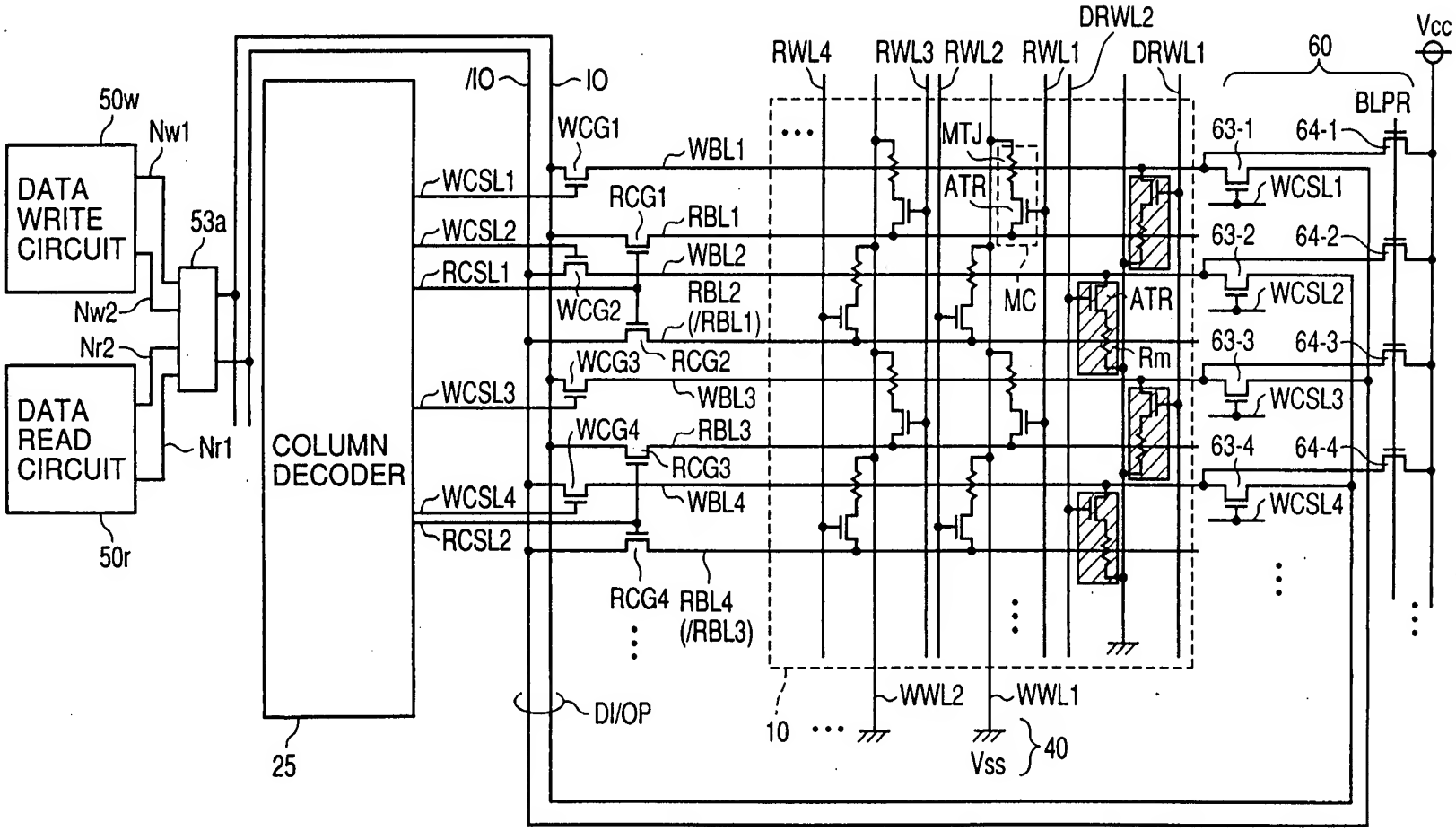
DATA WRITE CIRCUIT
DATA READ CIRCUIT
50w
50r
Nw1
Nw2
Nr2
Nr1
53a
COLUMN DECODER
25
/IO
IO
WCG1
WCG2
WCG3
WCG4
WCSL1
WCSL2
WCSL3
WCSL4
RCSL1
RCSL2
WBL1
WBL2
WBL3
WBL4
RCG1
RCG2
RCG3
RCG4
RBL1
RBL2
(/RBL1)
RBL3
RBL4
(/RBL3)
DI/OP
RWL4
RWL3
RWL2
RWL1
DRWL2
DRWL1
MTJ
ATR
MC
Rm
WWL2
WWL1
10
Vss
40
60
Vcc
BLPR
63-1
64-1
63-2
64-2
63-3
64-3
63-4
64-4

FIG.87

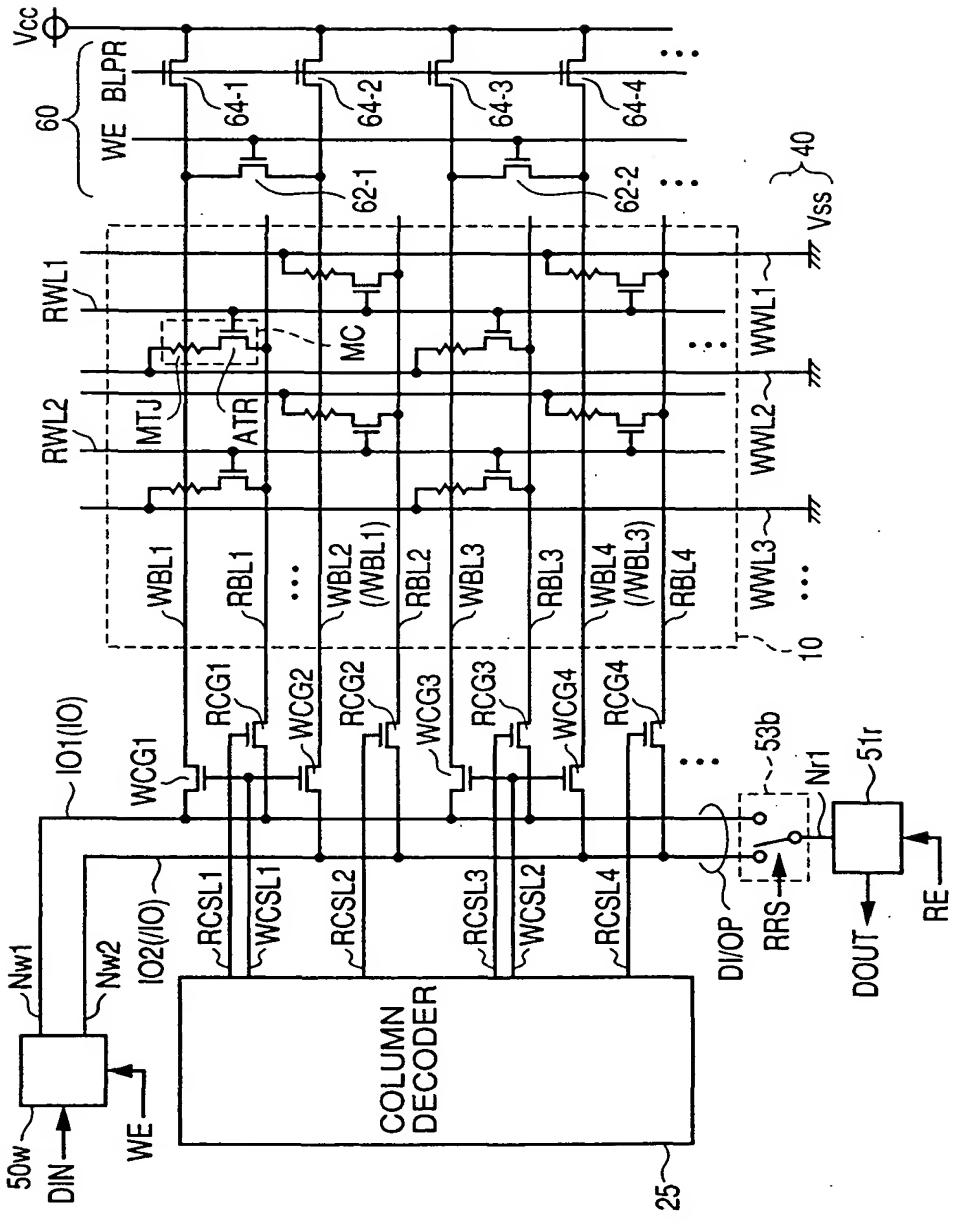
Vcc
60
WE
BLPR
64-1
64-2
64-3
64-4
62-1
62-2
40
Vss
RWL1
RWL2
MTJ
ATR
MC
WWL1
WWL2
WWL3
WBL1
RBL1
WBL2 (/WBL1)
RBL2
WBL3
RBL3
WBL4 (/WBL3)
RBL4
10
IO1(IO)
IO2(/IO)
WCG1
RCG1
WCG2
RCG2
WCG3
RCG3
WCG4
RCG4
RCSL1
WCSL1
RCSL2
RCSL3
WCSL2
RCSL4
53b
Nr1
51r
DI/OP
RRS
DOUT
RE
Nw1
Nw2
50w
DIN
WE
COLUMN DECODER
25

FIG.88 PRIOR ART

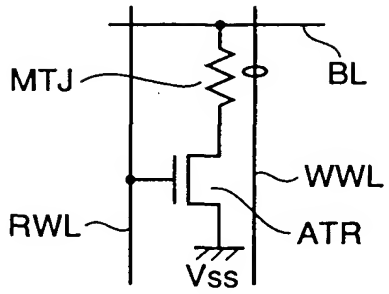

FIG.89 PRIOR ART

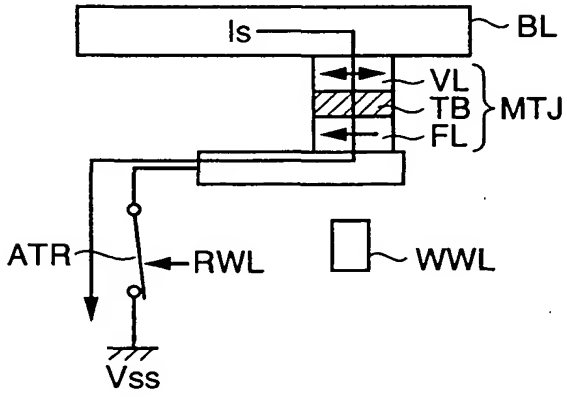

FIG.90 PRIOR ART

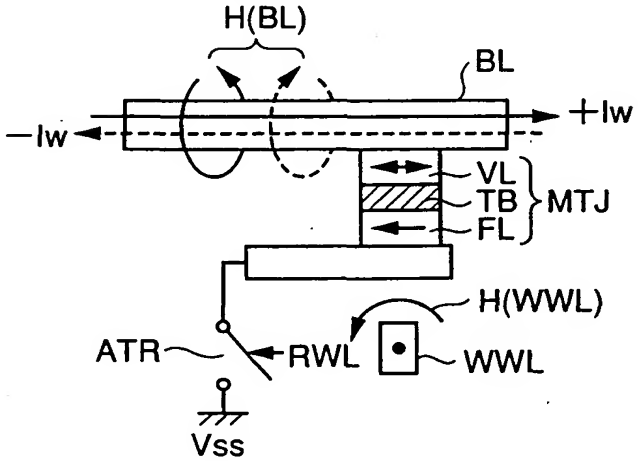

FIG.91 PRIOR ART

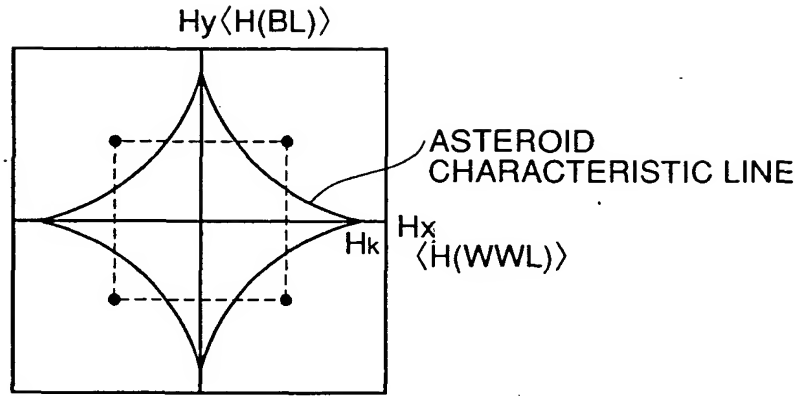

FIG.92 PRIOR ART

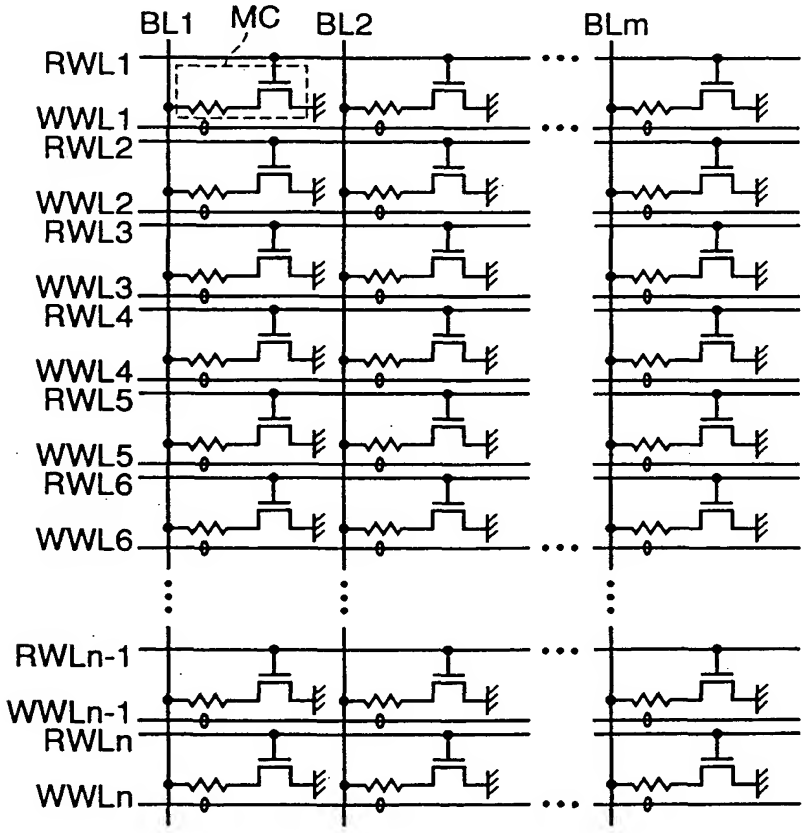

FIG.93 PRIOR ART